tide GPT-char

Lucy Score = Throughput x Availability x Acc / 10,000. LPD condenses live-fit vs Acc-champ RAM.
[T]=Tween [S]=Split [FP]=FastProxy [L]=Linear [HP]=HeadProxy
done - epoch 1 - lr 200 - 2026-08-21 16:25:28 - 0.0.0.0:8155
This epoch 986 / 986 cells. Recorded 986 results. Learning rate 200.
Score 0 usually means the cell finished before a Lucy pulse (Acc never sampled). Score is live-fit: Throughput x Availability x Acc.
SGD that blocks serve dies on Availability. SoftAcc is serve-confidence only.
live_gpt v1.0.0 - cameralx5 - tinyshakespeare - 4096 windows - seq 32 - causal MHA - A->B->A2 - SIMD

Lucy champions (this tide)

Axis	Cell	Score	Soft	Acc	Thru	Avail
hard acc	uint5|none|Mesh[T]Alt|cameralx5|simd	1.03	6.3	7.8	83.6	15.7
throughput	float32|none|Mesh[T][S]Sparse|cameralx5|simd	8.53	0.0	2.5	945.0	36.0
availability	int|none|[T][S][L]Cache|cameralx5|simd	4.50	1.6	2.6	458.3	37.4
lucy score	binary|none|[T][S][L]Cache|cameralx5|simd	28.80	4.9	9.2	878.5	35.6
mobile score (trap)	binary|none|[T][S][L]Cache|cameralx5|simd	28.80	4.9	9.2	878.5	35.6
acc/sec	binary|none|[T][S][L]Cache|cameralx5|simd	28.80	4.9	9.2	878.5	35.6

Lucy axis champions (this tide)

Axis	Mode	DType	Arch	Value
hard_acc	Step[T][S][HP]	int	cameralx5	10.83
throughput	Mesh[T][S]Sparse	float32	cameralx5	944.96
availability	[T][S][L]Cache	int	cameralx5	37.43
score	[T][S][L]Cache	binary	cameralx5	28.80
soft_acc	Mesh[T]Alt	uint5	cameralx5	6.31
acc_thru	[T][S][L]Cache	binary	cameralx5	80.82
realtime	Mesh[T][S]Sparse	float32	cameralx5	340.28
adapt	[T]Alt	uint3	cameralx5	6.81
keep_learn	[T][S]Sparse	binary	cameralx5	10.73
acc_per_sec	[T][S][L]Cache	binary	cameralx5	1.30
consistency	[T]Alt	int6	cameralx5	12.37
stability	sgd	fp4	cameralx5	100.00
mobile_score	[T][S][L]Cache	binary	cameralx5	2507.62
lpd	[T][S][L]Cache	binary	cameralx5	29.39
mspeed	[T][S][L]Cache	int8	cameralx5	1.00
mavail	[T][S][L]Cache	uint3	cameralx5	1.00
mix	[T][S][L]Cache	binary	cameralx5	0.92
gold_std	[T][S][L]Cache	binary	cameralx5	11.76

Best settings per train mode

Mode	DType	Format	Score	Soft	Acc	Avail	n
[T][S][L]Cache	binary	none	28.8	4.9	9.2	35.6	34
[T][S]Sparse	int4	none	21.9	4.3	7.2	35.3	34
Mesh[T][S]Sparse	int2	none	21.7	4.5	7.2	35.0	34
[T][S][L]	int4	none	21.1	4.9	7.8	33.8	34
Step[T][S][L]Cache	float32	none	18.0	2.3	9.4	29.8	34
Step[T][S][L]	float32	none	16.2	2.0	8.3	29.9	34
step_sgd	int8	none	10.6	4.4	6.8	26.2	34
[T][S][FP]	int8	none	9.7	4.2	7.0	26.2	34
Mesh[T][S][FP]	uint8	none	9.6	4.9	7.6	26.6	34
Step[T][S][HP]	float32	none	9.0	2.1	8.9	23.0	34
step_tween	float32	none	8.8	1.8	8.6	22.1	34

step_tween_chain	uint8	none	8.8	4.3	7.0	25.6	34
Step[T][S][HP]Async	float32	none	8.7	2.1	8.6	23.1	34
[T][S][HP]	int8	none	8.7	4.1	6.1	26.2	34
Step[T][S][FP]	float32	none	8.5	2.2	8.9	22.4	34
Step[T][S]Sparse	float32	none	8.5	2.2	8.9	22.4	34
tween	float32	none	8.4	2.0	9.6	20.6	34
sgd	uint8	none	8.1	4.4	7.5	23.5	34
Step[T][S]	float32	none	8.1	2.0	7.7	23.0	34
[T][S][HP]Async	uint8	none	7.9	3.2	6.3	26.5	34
Mesh[T]	float32	none	7.7	2.0	9.8	20.1	34
[T][S]	int8	none	7.6	4.0	5.2	26.2	34
MeshBP	int8	none	7.3	4.7	7.5	22.0	34
tween_chain	uint8	none	7.1	4.3	7.0	23.4	34
Mesh[T][S]	int8	none	6.9	4.2	5.1	25.7	34
Mesh[T]Chain	uint8	none	6.5	4.4	7.2	22.8	34
Step[T]Alt	float32	none	4.0	2.4	8.3	16.6	34
[T]Alt	float32	none	3.2	0.0	2.9	22.8	34
Mesh[T]Alt	float32	none	2.7	0.0	2.6	22.5	34

Best dtype per mode

Mode	Winner dtype	Score	Soft	Acc
[T][S][L]Cache	binary	28.8	4.9	9.2
[T][S]Sparse	int4	21.9	4.3	7.2
Mesh[T][S]Sparse	int2	21.7	4.5	7.2
[T][S][L]	int4	21.1	4.9	7.8
Step[T][S][L]Cache	float32	18.0	2.3	9.4
Step[T][S][L]	float32	16.2	2.0	8.3
step_sgd	int8	10.6	4.4	6.8
[T][S][FP]	int8	9.7	4.2	7.0
Mesh[T][S][FP]	uint8	9.6	4.9	7.6
Step[T][S][HP]	float32	9.0	2.1	8.9
step_tween	float32	8.8	1.8	8.6
step_tween_chain	uint8	8.8	4.3	7.0
Step[T][S][HP]Async	float32	8.7	2.1	8.6
[T][S][HP]	int8	8.7	4.1	6.1
Step[T][S][FP]	float32	8.5	2.2	8.9
Step[T][S]Sparse	float32	8.5	2.2	8.9
tween	float32	8.4	2.0	9.6
sgd	uint8	8.1	4.4	7.5
Step[T][S]	float32	8.1	2.0	7.7
[T][S][HP]Async	uint8	7.9	3.2	6.3
Mesh[T]	float32	7.7	2.0	9.8
[T][S]	int8	7.6	4.0	5.2
MeshBP	int8	7.3	4.7	7.5
tween_chain	uint8	7.1	4.3	7.0
Mesh[T][S]	int8	6.9	4.2	5.1
Mesh[T]Chain	uint8	6.5	4.4	7.2
Step[T]Alt	float32	4.0	2.4	8.3
[T]Alt	float32	3.2	0.0	2.9
Mesh[T]Alt	float32	2.7	0.0	2.6

Best mode per dtype

DType	Winner mode	Score	Soft	Acc
binary	[T][S][L]Cache	28.8	4.9	9.2
int4	[T][S][L]Cache	28.8	4.7	8.7
ternary	[T][S][L]Cache	28.4	4.8	8.7
int8	[T][S][L]Cache	27.9	4.6	8.4
int2	[T][S][L]Cache	27.2	4.7	8.9
uint8	[T][S][L]Cache	25.0	4.7	8.2
float32	Step[T][S][L]Cache	18.0	2.3	9.4
uint16	[T][S][L]Cache	17.0	4.8	8.5
int16	[T][S][L]Cache	16.5	4.9	8.5
uint32	[T][S][L]Cache	16.3	4.6	8.2
uint64	[T][S][L]Cache	16.2	4.7	8.0
uint4	[T][S][L]Cache	15.4	4.5	7.5
uint2	[T][S][L]Cache	15.1	4.6	7.9
int32	[T][S][L]Cache	14.8	4.6	7.7
uintptr	[T][S][L]Cache	14.5	4.8	8.2
uint	[T][S][L]Cache	13.9	4.8	7.8
float64	Step[T][S][L]Cache	13.3	2.1	9.2
bfloat16	Step[T][S][L]Cache	12.7	1.7	8.5
nf4	[T][S][L]Cache	12.7	4.6	8.5
uint3	[T][S][L]Cache	10.9	4.7	8.3
int64	Step[T][S][L]Cache	10.8	2.4	9.3
float16	Step[T][S][L]	10.3	2.1	8.7
int3	[T][S][L]Cache	10.0	4.7	8.1
fp8e5m2	Step[T][S][L]	9.2	1.9	7.9
fp8e4m3	Step[T][S][L]	9.0	1.9	9.1
int	Step[T][S][L]	9.0	2.2	9.7
complex128	Step[T][S][L]Cache	8.6	2.1	9.0
complex64	Step[T][S][L]	8.6	2.4	8.9
uint5	[T][S][L]Cache	8.4	4.6	7.8
int5	[T][S][L]Cache	8.0	4.7	7.8
uint6	[T][S][L]Cache	7.4	4.7	7.5
fp4	[T][S][L]	7.3	1.5	3.0
int6	[T][S][L]Cache	7.3	4.6	7.7
fp6	[T][S][L]Cache	7.0	4.5	7.5

Leaderboard (Lucy Score)

#	Cell	Score	Soft	Acc	Thru	Avail
1	binary|none|[T][S][L]Cache|cameralx5|simd	28.8	4.9	9.2	878.5	35.6
2	int4|none|[T][S][L]Cache|cameralx5|simd	28.8	4.7	8.7	910.7	36.3
3	ternary|none|[T][S][L]Cache|cameralx5|simd	28.4	4.8	8.7	901.1	36.2
4	int8|none|[T][S][L]Cache|cameralx5|simd	27.9	4.6	8.4	920.8	36.2
5	int2|none|[T][S][L]Cache|cameralx5|simd	27.2	4.7	8.9	868.2	35.1
6	uint8|none|[T][S][L]Cache|cameralx5|simd	25.0	4.7	8.2	826.4	36.7
7	int4|none|[T][S]Sparse|cameralx5|simd	21.9	4.3	7.2	868.1	35.3
8	int2|none|Mesh[T][S]Sparse|cameralx5|simd	21.7	4.5	7.2	856.0	35.0
9	ternary|none|Mesh[T][S]Sparse|cameralx5|simd	21.4	4.2	7.0	862.7	35.2
10	int2|none|[T][S]Sparse|cameralx5|simd	21.2	4.4	7.0	855.3	35.4
11	int4|none|[T][S][L]|cameralx5|simd	21.1	4.9	7.8	805.0	33.8
12	binary|none|[T][S]Sparse|cameralx5|simd	20.5	4.2	6.6	879.1	35.6
13	int8|none|[T][S][L]|cameralx5|simd	20.4	4.5	7.2	831.8	34.2
14	ternary|none|[T][S][L]|cameralx5|simd	19.8	4.5	7.3	802.5	33.6

15	ternary|none|[T][S]Sparse|cameralx5|simd	19.6	3.4	6.5	858.9	35.1
16	int8|none|[T][S]Sparse|cameralx5|simd	19.5	3.7	6.1	893.4	35.5
17	uint8|none|[T][S]Sparse|cameralx5|simd	18.7	3.7	6.4	801.5	36.2
18	int4|none|Mesh[T][S]Sparse|cameralx5|simd	18.3	3.9	5.9	871.4	35.6
19	float32|none|Step[T][S][L]Cache|cameralx5|simd	18.0	2.3	9.4	642.6	29.8
20	binary|none|[T][S][L]|cameralx5|simd	17.9	4.7	6.8	785.0	33.3

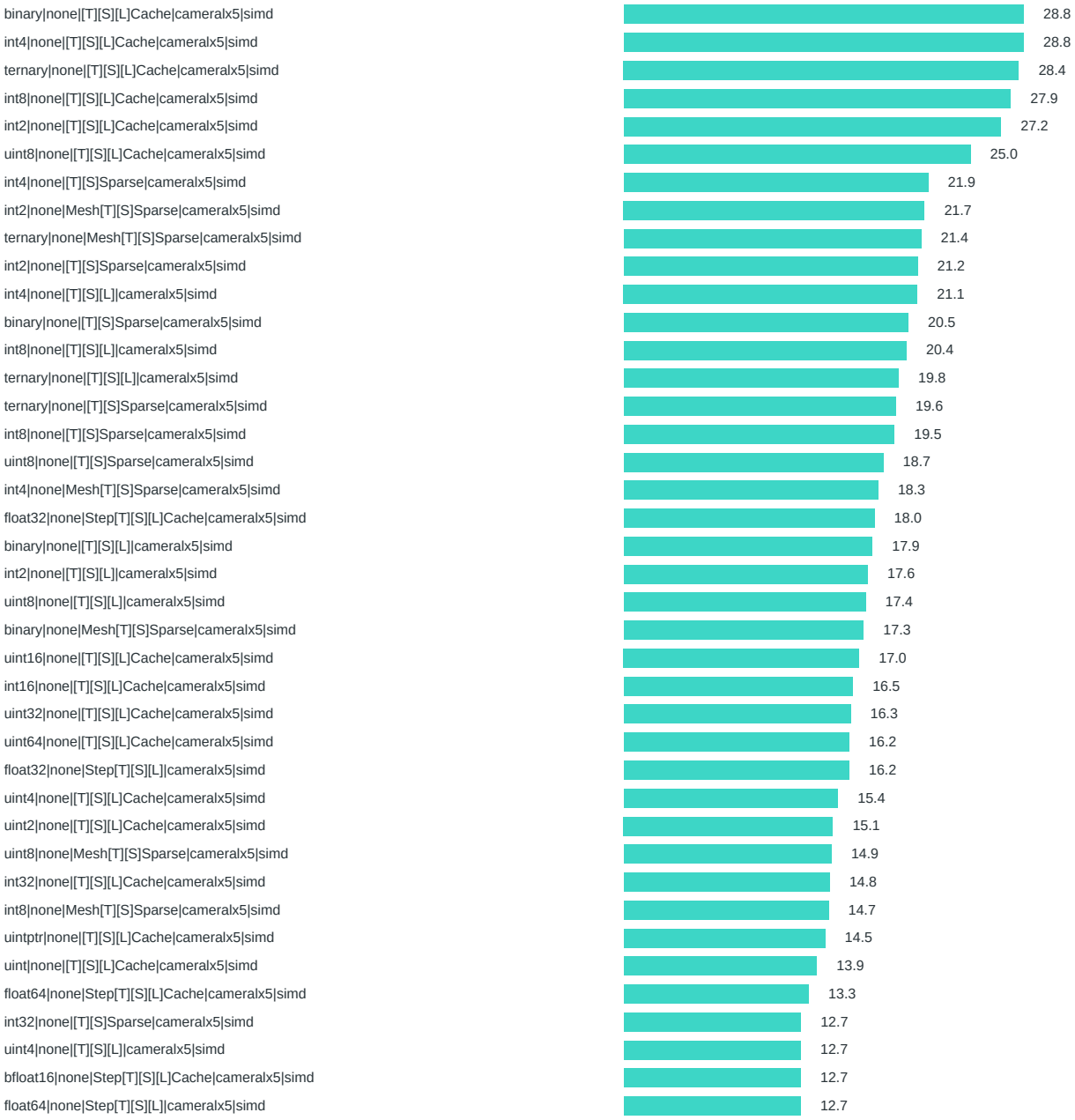
Leaderboard (SoftAcc)

#	Cell	Score	Soft	Acc	Thru	Avail
1	int4|none|[T][S][L]|cameralx5|simd	21.1	4.9	7.8	805.0	33.8
2	binary|none|[T][S][L]Cache|cameralx5|simd	28.8	4.9	9.2	878.5	35.6
3	int16|none|[T][S][L]Cache|cameralx5|simd	16.5	4.9	8.5	524.5	37.2
4	uintptr|none|[T][S][L]Cache|cameralx5|simd	14.5	4.8	8.2	475.6	36.9
5	uint16|none|[T][S][L]Cache|cameralx5|simd	17.0	4.8	8.5	543.0	36.6
6	ternary|none|[T][S][L]Cache|cameralx5|simd	28.4	4.8	8.7	901.1	36.2
7	uint|none|[T][S][L]Cache|cameralx5|simd	13.9	4.8	7.8	479.2	37.1
8	int4|none|[T][S][L]Cache|cameralx5|simd	28.8	4.7	8.7	910.7	36.3
9	uint64|none|[T][S][L]Cache|cameralx5|simd	16.2	4.7	8.0	549.6	36.9
10	int2|none|[T][S][L]Cache|cameralx5|simd	27.2	4.7	8.9	868.2	35.1
11	uint8|none|[T][S][L]Cache|cameralx5|simd	25.0	4.7	8.2	826.4	36.7
12	binary|none|[T][S][L]|cameralx5|simd	17.9	4.7	6.8	785.0	33.3
13	uint4|none|[T][S][L]|cameralx5|simd	12.7	4.6	7.0	511.1	35.7
14	int32|none|[T][S][L]Cache|cameralx5|simd	14.8	4.6	7.7	520.1	37.1
15	uint32|none|[T][S][L]Cache|cameralx5|simd	16.3	4.6	8.2	544.2	36.8
16	int8|none|[T][S][L]Cache|cameralx5|simd	27.9	4.6	8.4	920.8	36.2
17	uint2|none|[T][S][L]Cache|cameralx5|simd	15.1	4.6	7.9	515.6	36.7
18	int2|none|[T][S][L]|cameralx5|simd	17.6	4.5	6.9	778.6	32.9
19	ternary|none|[T][S][L]|cameralx5|simd	19.8	4.5	7.3	802.5	33.6
20	uint8|none|[T][S][L]|cameralx5|simd	17.4	4.5	7.0	728.5	34.3

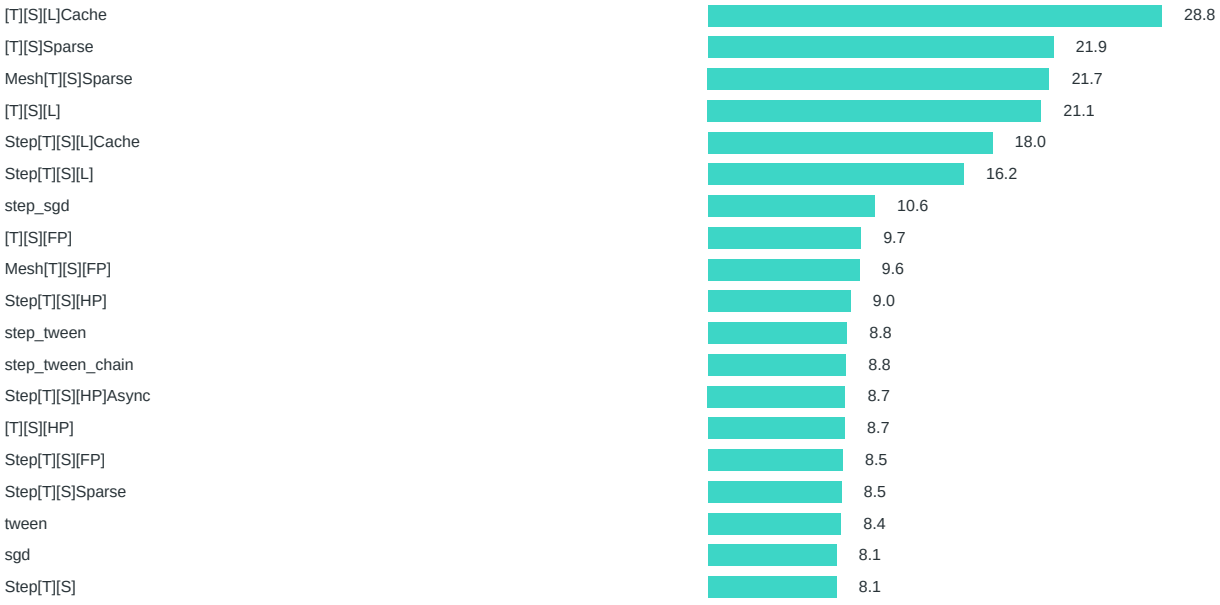
Leaderboard (hard Acc)

#	Cell	Score	Soft	Acc	Thru	Avail
1	float32|none|Step[T][S][L]Cache|cameralx5|simd	18.0	2.3	9.4	642.6	29.8
2	binary|none|[T][S][L]Cache|cameralx5|simd	28.8	4.9	9.2	878.5	35.6
3	float64|none|Step[T][S][L]Cache|cameralx5|simd	13.3	2.1	9.2	479.1	30.3
4	int2|none|[T][S][L]Cache|cameralx5|simd	27.2	4.7	8.9	868.2	35.1
5	float64|none|Step[T][S][L]|cameralx5|simd	12.7	2.2	8.8	479.3	30.3
6	ternary|none|[T][S][L]Cache|cameralx5|simd	28.4	4.8	8.7	901.1	36.2
7	int4|none|[T][S][L]Cache|cameralx5|simd	28.8	4.7	8.7	910.7	36.3
8	bfloat16|none|Step[T][S][L]Cache|cameralx5|simd	12.7	1.7	8.5	492.9	30.2
9	uint16|none|[T][S][L]Cache|cameralx5|simd	17.0	4.8	8.5	543.0	36.6
10	int16|none|[T][S][L]Cache|cameralx5|simd	16.5	4.9	8.5	524.5	37.2
11	int8|none|[T][S][L]Cache|cameralx5|simd	27.9	4.6	8.4	920.8	36.2
12	float32|none|Step[T][S][L]|cameralx5|simd	16.2	2.0	8.3	652.4	29.9
13	uintptr|none|[T][S][L]Cache|cameralx5|simd	14.5	4.8	8.2	475.6	36.9
14	uint8|none|[T][S][L]Cache|cameralx5|simd	25.0	4.7	8.2	826.4	36.7
15	uint32|none|[T][S][L]Cache|cameralx5|simd	16.3	4.6	8.2	544.2	36.8
16	uint64|none|[T][S][L]Cache|cameralx5|simd	16.2	4.7	8.0	549.6	36.9
17	uint2|none|[T][S][L]Cache|cameralx5|simd	15.1	4.6	7.9	515.6	36.7
18	uint|none|[T][S][L]Cache|cameralx5|simd	13.9	4.8	7.8	479.2	37.1
19	int4|none|[T][S][L]|cameralx5|simd	21.1	4.9	7.8	805.0	33.8
20	int32|none|[T][S][L]Cache|cameralx5|simd	14.8	4.6	7.7	520.1	37.1

Top scores



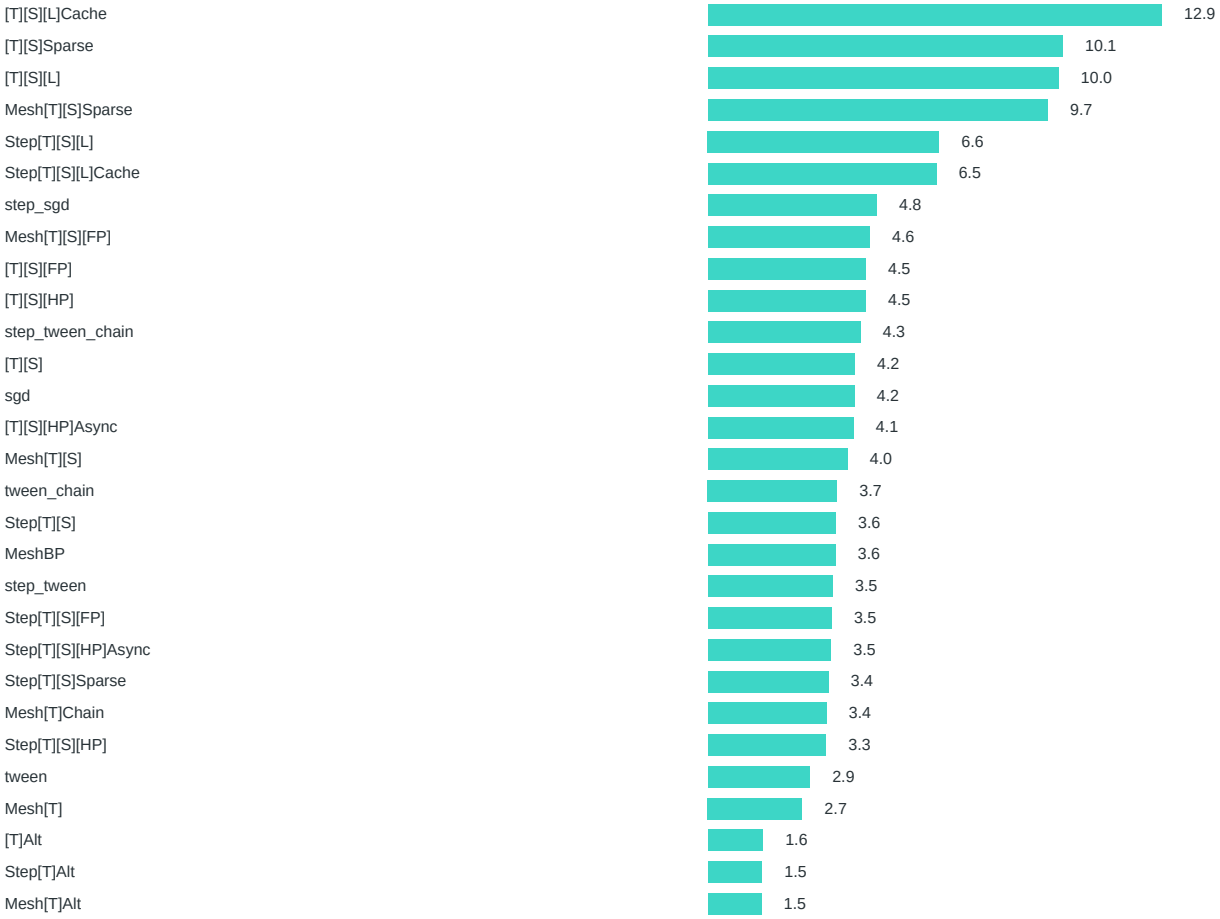
Best settings per mode



Best settings per mode



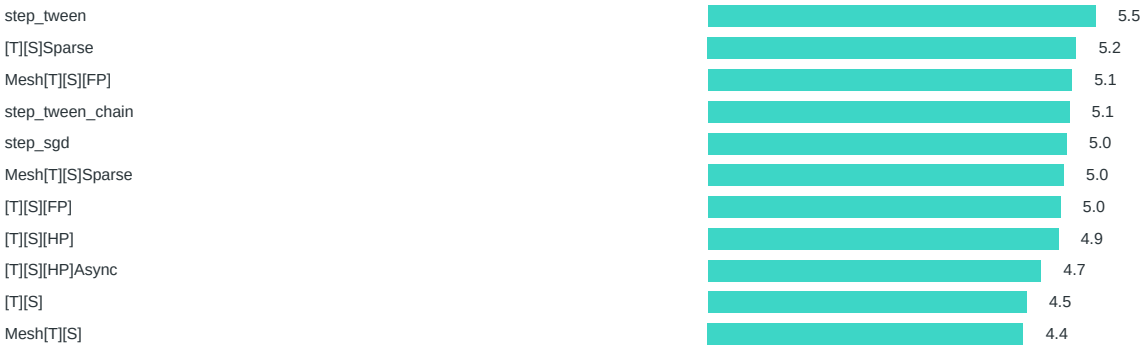
Mean Score by train mode



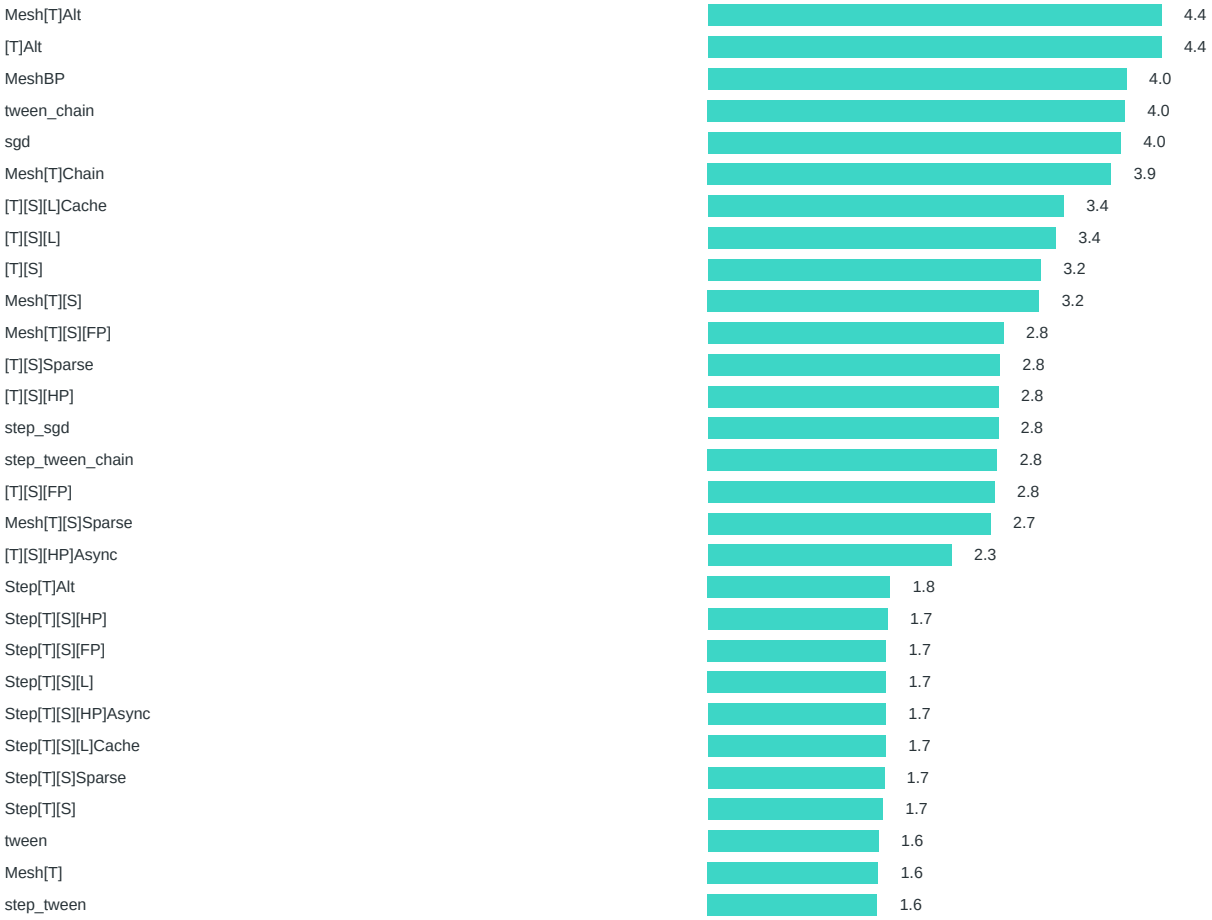
Mean hard Acc by train mode



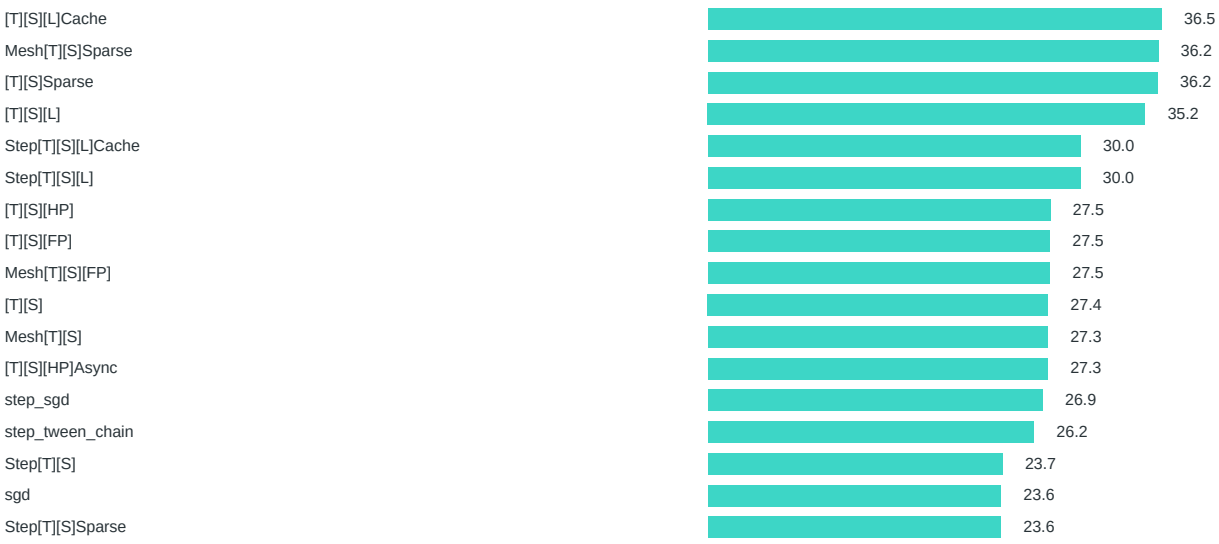
Mean hard Acc by train mode



Mean SoftAcc by train mode



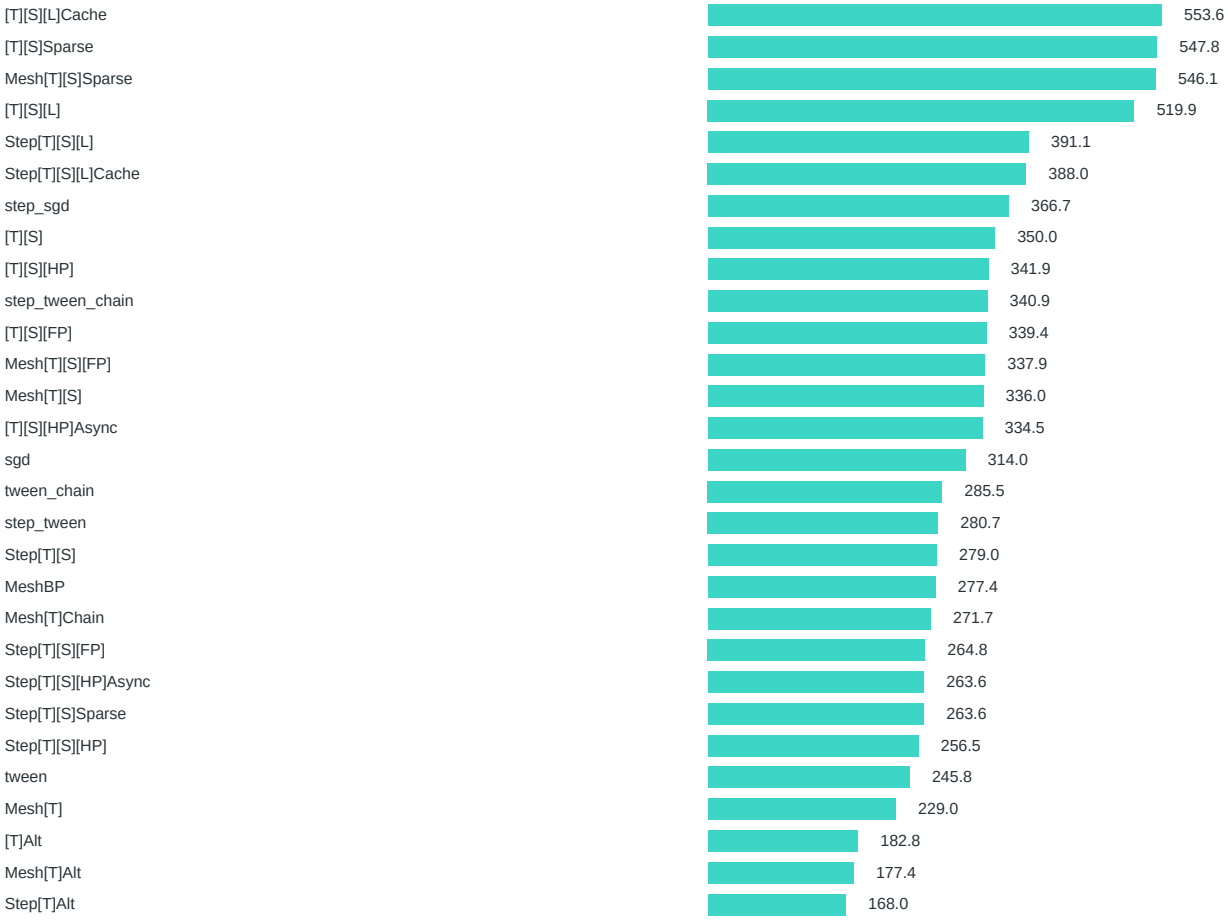
Mean Availability by train mode



Mean Availability by train mode



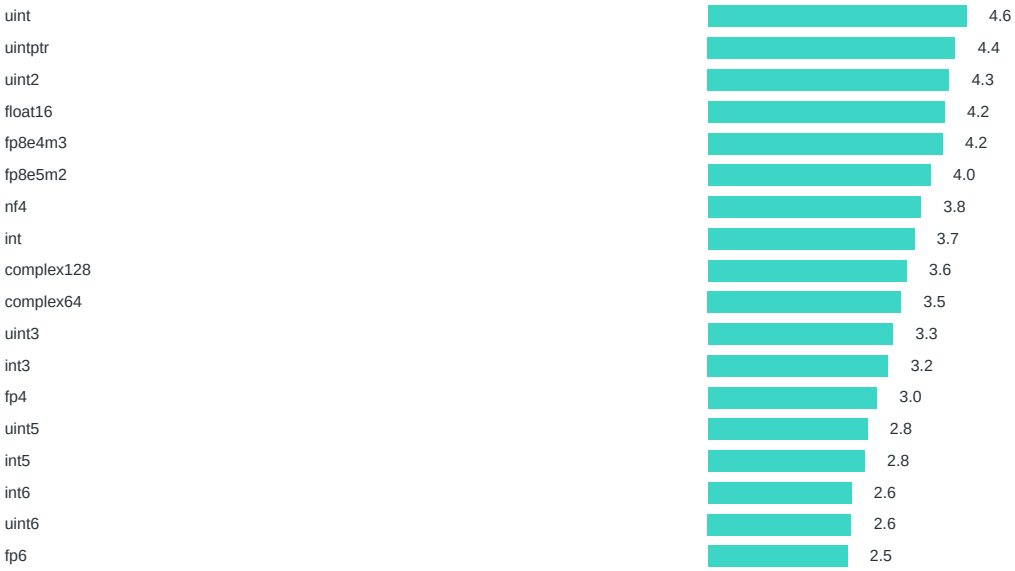
Mean Throughput by train mode



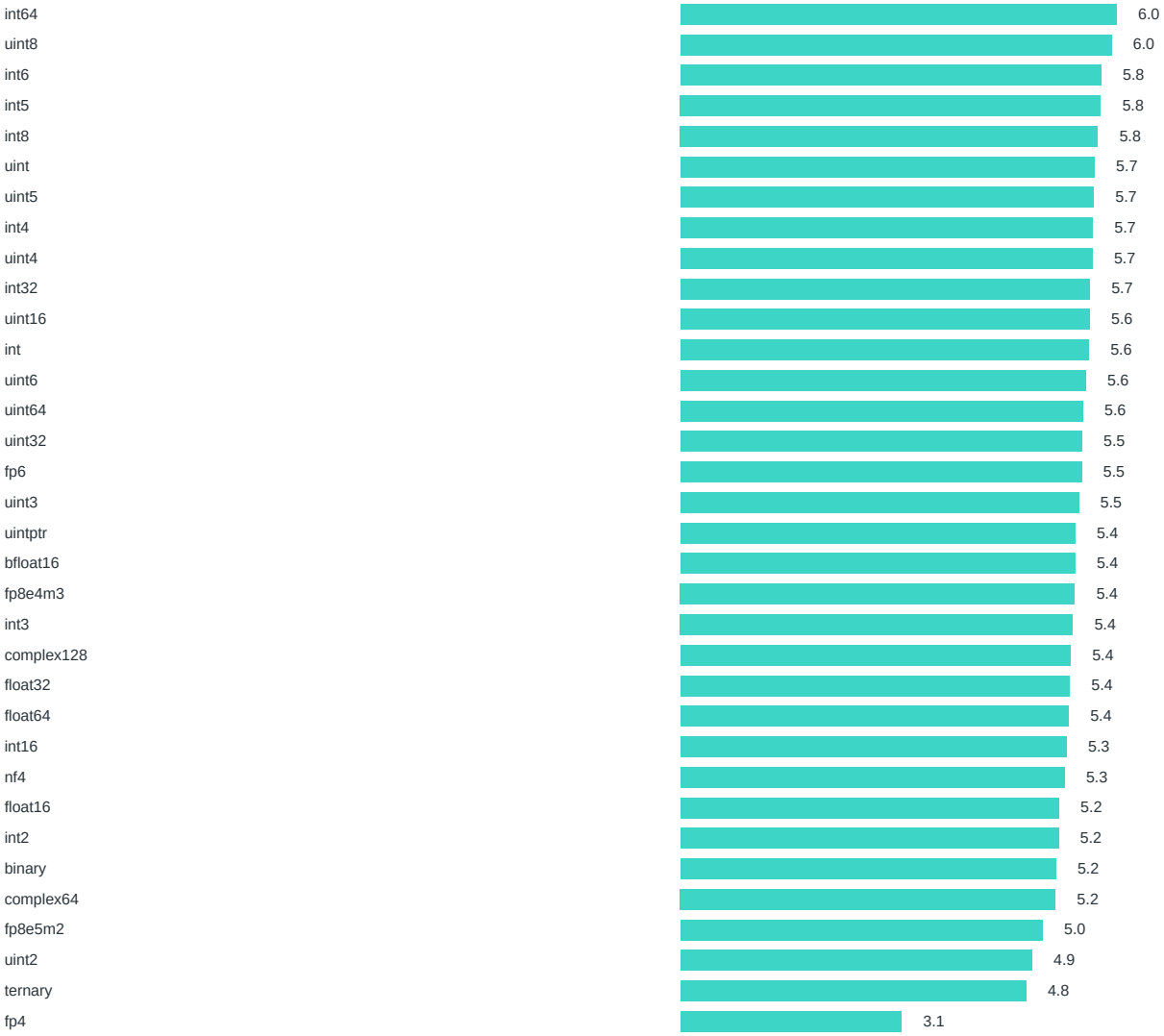
Mean Score by dtype



Mean Score by dtype



Mean hard Acc by dtype



Mean Score by arch



Honesty - mean Score, every mode x dtype (cols 1-12)

Honesty - mean Score, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	4	6	3	3	2	6	4	2	2	3	2	3
Mesh[T]	6	1	4	3	4	8	6	1	1	4	3	4
Mesh[T]Alt	2	2	1	1	2	3	2	2	1	1	2	1
Mesh[T]Chain	4	3	3	3	4	6	5	2	2	2	3	1
Mesh[T][S]	3	6	2	2	2	4	4	4	2	5	2	4
Mesh[T][S][FP]	3	7	2	3	3	4	3	3	3	3	2	2
Mesh[T][S]Sparse	7	17	4	4	5	9	7	7	6	8	6	4
Step[T]Alt	3	1	2	2	3	4	3	1	0	2	2	2
Step[T][S]	7	4	5	5	6	8	7	2	2	5	6	5
Step[T][S][FP]	7	3	5	4	6	9	8	2	2	4	6	4
Step[T][S][HP]	7	3	4	4	6	9	8	2	1	4	5	6
Step[T][S][HP]Async	6	4	5	5	6	9	7	2	1	5	4	4
Step[T][S][L]	11	8	8	9	10	16	13	4	3	9	9	9
Step[T][S][L]Cache	13	8	9	8	10	18	13	4	2	8	9	9
Step[T][S]Sparse	8	4	5	5	5	8	6	2	1	4	5	5
[T]Alt	2	2	1	1	1	3	2	2	1	1	1	1
[T][S]	3	7	2	2	3	4	3	4	2	5	3	4
[T][S][FP]	3	7	2	2	2	4	3	3	3	2	3	2
[T][S][HP]	3	6	2	2	2	4	3	3	3	2	3	2
[T][S][HP]Async	3	7	2	2	3	4	3	3	2	3	2	2
[T][S][L]	6	18	4	4	5	9	7	7	6	9	5	4
[T][S][L]Cache	7	29	4	4	5	8	7	6	7	5	5	4
[T][S]Sparse	7	20	4	5	5	8	7	6	6	7	6	5
sgd	5	6	3	1	4	7	5	2	1	4	4	3
step_sgd	3	8	2	2	3	4	4	3	3	3	3	2
step_tween	7	1	6	5	5	9	7	2	1	5	4	5
step_tween_chain	3	5	2	2	3	3	3	3	3	3	2	2
tween	6	1	4	4	5	8	6	2	1	3	4	4
tween_chain	5	3	3	2	3	6	5	2	2	4	4	3

Honesty - mean Score, every mode x dtype (cols 13-24)

Honesty - mean Score, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	2	7	3	4	4	2	2	4	7	3	5	3
Mesh[T]	2	1	1	2	3	1	1	5	5	2	1	2
Mesh[T]Alt	2	2	1	2	2	1	1	1	2	1	2	1
Mesh[T]Chain	3	6	2	3	6	1	2	3	6	3	5	3
Mesh[T][S]	4	5	3	5	5	3	2	4	7	3	6	5
Mesh[T][S][FP]	5	7	5	5	6	4	3	2	8	5	8	6
Mesh[T][S]Sparse	11	22	7	11	18	5	6	9	15	8	21	11
Step[T]Alt	2	1	1	1	1	1	1	3	2	1	1	1
Step[T][S]	3	3	2	3	5	2	2	6	5	2	2	3
Step[T][S][FP]	3	2	2	3	4	2	2	6	4	2	2	2
Step[T][S][HP]	3	2	2	3	3	1	2	5	4	2	1	3
Step[T][S][HP]Async	3	2	2	3	4	2	1	6	5	2	3	2
Step[T][S][L]	5	6	3	6	8	3	3	11	7	4	6	5
Step[T][S][L]Cache	5	5	3	6	9	3	2	11	9	4	4	5
Step[T][S]Sparse	3	2	2	3	4	1	1	6	4	2	2	2
[T]Alt	2	2	1	2	2	1	1	1	2	1	2	2
[T][S]	5	6	3	5	6	3	3	5	8	4	5	4
[T][S][FP]	5	8	4	5	8	4	4	2	10	3	6	5
[T][S][HP]	6	8	2	5	8	4	3	3	9	5	8	4
[T][S][HP]Async	3	7	4	5	7	3	3	3	7	5	7	5
[T][S][L]	13	18	8	12	21	6	6	5	20	9	20	11
[T][S][L]Cache	16	27	10	15	29	8	7	5	28	13	28	14
[T][S]Sparse	10	21	8	13	22	6	5	5	19	9	20	10
sgd	5	7	3	5	4	3	2	4	7	3	7	4
step_sgd	6	7	4	5	9	3	3	3	11	4	5	6
step_tween	3	2	1	3	5	2	1	6	6	2	2	3
step_tween_chain	6	7	4	5	8	3	3	3	7	4	4	5
tween	3	2	1	2	3	1	1	5	4	1	1	2
tween_chain	3	5	3	4	6	2	2	3	7	2	6	4

Honesty - mean Score, every mode x dtype (cols 25-34)

Honesty - mean Score, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	4	4	3	4	4	2	2	4	7	2
Mesh[T]	3	1	1	2	2	1	1	3	3	2
Mesh[T]Alt	2	2	1	2	2	1	1	2	2	2
Mesh[T]Chain	2	4	3	4	5	2	2	4	7	3
Mesh[T][S]	5	5	3	5	4	3	2	5	6	4
Mesh[T][S][FP]	7	6	4	6	5	2	3	6	10	5
Mesh[T][S]Sparse	13	9	7	11	11	7	6	12	15	9
Step[T]Alt	1	1	1	1	1	1	1	1	2	1
Step[T][S]	3	2	2	3	3	2	1	3	4	3
Step[T][S][FP]	3	2	2	3	3	2	2	3	4	3
Step[T][S][HP]	3	1	2	3	3	2	1	3	4	2
Step[T][S][HP]Async	3	2	2	3	3	2	2	3	4	2
Step[T][S][L]	7	2	3	5	5	3	2	5	9	5
Step[T][S][L]Cache	5	3	3	5	6	3	2	5	7	5
Step[T][S]Sparse	3	2	2	3	3	2	1	2	4	3
[T]Alt	2	2	1	2	2	1	1	2	2	1
[T][S]	5	5	3	5	5	3	2	4	6	5
[T][S][FP]	6	6	4	6	5	3	3	5	8	5
[T][S][HP]	6	6	5	4	5	4	3	4	8	5
[T][S][HP]Async	4	5	4	6	5	3	3	5	8	4
[T][S][L]	11	11	7	12	13	6	6	13	17	11
[T][S][L]Cache	17	15	11	16	15	8	7	16	25	14
[T][S]Sparse	12	10	8	12	11	7	6	13	19	11
sgd	5	4	3	5	5	3	2	3	8	2
step_sgd	6	6	4	6	6	3	3	7	9	5
step_tween	3	2	1	3	3	2	2	3	6	3
step_tween_chain	6	6	4	7	6	3	3	6	9	4
tween	3	1	1	3	2	1	1	3	4	2
tween_chain	4	2	3	2	5	2	2	4	7	4

Honesty - mean hard Acc, every mode x dtype (cols 1-12)

Honesty - mean hard Acc, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	5	7	5	5	3	5	5	3	6	5	4	6
Mesh[T]	10	2	9	9	9	10	9	3	5	11	8	9
Mesh[T]Alt	3	7	3	3	3	3	3	7	7	2	3	4
Mesh[T]Chain	6	3	6	5	6	5	6	3	7	4	5	2
Mesh[T][S]	3	5	3	3	3	3	3	4	5	5	2	5
Mesh[T][S][FP]	3	7	2	3	3	3	3	3	6	3	3	3
Mesh[T][S]Sparse	3	6	3	3	3	3	3	3	7	4	3	3
Step[T]Alt	9	5	9	9	10	8	7	3	4	8	8	9
Step[T][S]	8	5	9	9	8	8	8	3	4	9	8	8
Step[T][S][FP]	9	4	10	8	9	9	10	2	5	8	9	8
Step[T][S][HP]	10	4	8	8	10	9	9	3	4	8	9	11
Step[T][S][HP]Async	8	5	9	8	9	9	9	3	4	8	7	9
Step[T][S][L]	8	4	8	9	9	8	9	3	5	9	8	10
Step[T][S][L]Cache	9	5	9	8	8	9	9	3	5	8	8	9
Step[T][S]Sparse	10	4	9	9	8	9	7	3	5	7	8	9
[T]Alt	3	7	3	3	2	3	2	7	6	4	2	5
[T][S]	3	5	3	3	3	3	3	4	4	5	3	5
[T][S][FP]	3	6	2	3	2	3	3	2	7	2	3	3
[T][S][HP]	3	5	2	2	2	3	3	3	7	2	3	3
[T][S][HP]Async	3	6	2	3	3	3	2	3	5	3	3	3
[T][S][L]	2	7	3	3	3	3	3	3	7	5	3	3
[T][S][L]Cache	3	9	3	3	3	3	3	2	8	3	3	3
[T][S]Sparse	3	7	3	3	3	2	3	2	7	4	3	3
sgd	5	6	4	3	5	5	5	3	3	5	6	5
step_sgd	3	6	3	3	3	3	3	3	5	3	3	2
step_tween	9	2	10	10	8	9	8	3	5	9	7	9
step_tween_chain	3	5	3	3	3	2	3	2	6	3	2	2
tween	10	2	9	9	9	10	10	3	5	8	8	10
tween_chain	6	3	5	3	5	6	6	3	6	6	6	6

Honesty - mean hard Acc, every mode x dtype (cols 13-24)

Honesty - mean hard Acc, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	3	8	7	7	5	6	7	6	7	7	7	6
Mesh[T]	5	2	3	5	4	5	5	10	6	4	2	5
Mesh[T]Alt	7	7	7	7	7	7	7	5	7	6	7	7
Mesh[T]Chain	4	7	6	5	7	4	7	5	6	7	6	5
Mesh[T][S]	4	4	5	5	5	5	5	4	5	4	5	6
Mesh[T][S][FP]	5	7	7	5	5	7	6	3	6	7	7	7
Mesh[T][S]Sparse	6	7	6	6	6	5	6	5	5	5	7	6
Step[T]Alt	6	3	4	4	4	4	5	10	5	4	2	4
Step[T][S]	5	3	4	4	5	5	5	9	4	4	2	4
Step[T][S][FP]	4	2	4	5	5	5	5	10	4	5	3	4
Step[T][S][HP]	5	3	4	5	4	5	5	9	5	5	2	5
Step[T][S][HP]Async	5	3	4	5	5	5	5	10	6	4	3	4
Step[T][S][L]	4	3	4	5	4	5	5	10	4	5	3	5
Step[T][S][L]Cache	4	3	5	5	5	5	4	9	5	4	2	5
Step[T][S]Sparse	4	3	4	5	4	4	4	10	4	4	3	4
[T]Alt	8	6	7	7	7	7	7	5	6	8	6	8
[T][S]	5	5	5	5	5	6	5	5	5	5	4	5
[T][S][FP]	6	7	6	6	7	7	7	3	7	3	5	6
[T][S][HP]	6	7	3	6	7	7	6	3	6	6	7	5
[T][S][HP]Async	3	6	6	6	6	7	5	3	6	7	6	6
[T][S][L]	7	7	8	6	8	7	7	3	7	7	7	7
[T][S][L]Cache	8	9	8	8	9	8	8	3	8	9	9	8
[T][S]Sparse	6	7	7	7	7	6	6	3	6	6	6	6
sgd	7	8	6	7	4	7	7	6	6	6	7	6
step_sgd	6	6	7	5	7	7	6	3	7	5	4	7
step_tween	5	2	2	5	5	6	5	9	6	4	2	4
step_tween_chain	6	7	7	5	7	6	6	3	6	5	4	6
tween	6	3	3	4	5	5	5	10	5	3	2	5
tween_chain	5	7	7	6	6	7	6	5	7	3	7	7

Honesty - mean hard Acc, every mode x dtype (cols 25-34)

Honesty - mean hard Acc, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	7	6	7	6	7	6	7	7	7	4
Mesh[T]	5	2	3	5	5	5	5	6	4	5
Mesh[T]Alt	7	7	7	7	7	8	7	7	7	8
Mesh[T]Chain	3	7	7	6	7	6	6	7	7	5
Mesh[T][S]	5	6	4	5	5	5	5	5	4	5
Mesh[T][S][FP]	7	7	7	6	6	5	6	6	8	5
Mesh[T][S]Sparse	7	5	6	6	6	7	6	6	5	5
Step[T]Alt	4	2	5	4	5	4	4	4	5	5
Step[T][S]	4	3	5	4	5	4	4	5	5	5
Step[T][S][FP]	4	2	4	5	5	5	5	4	5	5
Step[T][S][HP]	5	2	4	4	5	5	5	5	5	5
Step[T][S][HP]Async	5	3	4	5	5	5	5	4	5	4
Step[T][S][L]	6	2	5	5	4	5	4	5	5	5
Step[T][S][L]Cache	5	3	4	4	5	5	4	4	4	5
Step[T][S]Sparse	5	3	4	4	5	5	4	4	5	5
[T]Alt	7	7	7	7	7	7	7	7	7	6
[T][S]	6	5	5	5	5	5	4	5	4	5
[T][S][FP]	6	6	6	7	5	6	5	5	6	7
[T][S][HP]	6	7	7	5	6	6	7	4	6	6
[T][S][HP]Async	4	6	7	6	5	6	5	6	6	6
[T][S][L]	6	6	7	7	7	7	7	7	7	7
[T][S][L]Cache	9	8	8	8	7	8	8	8	8	8
[T][S]Sparse	6	5	6	6	6	6	6	7	6	6
sgd	6	7	6	7	7	7	7	4	7	3
step_sgd	6	6	6	6	6	6	7	6	6	6
step_tween	4	2	3	5	4	5	5	5	6	4
step_tween_chain	7	7	6	7	6	6	6	7	7	6
tween	6	2	2	5	4	5	5	5	5	5
tween_chain	6	3	6	3	7	7	7	6	7	7

Honesty - mean SoftAcc, every mode x dtype (cols 1-12)

Honesty - mean SoftAcc, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	5	4	5	5	0	5	5	2	4	5	2	6
Mesh[T]	2	2	2	2	2	2	2	2	2	2	2	2
Mesh[T]Alt	0	6	0	0	0	0	0	5	6	2	0	4
Mesh[T]Chain	6	1	6	5	6	5	6	2	4	4	4	2
Mesh[T][S]	0	4	0	0	0	0	0	4	4	5	0	5
Mesh[T][S][FP]	0	4	0	0	0	0	0	2	4	2	0	2
Mesh[T][S]Sparse	0	3	0	0	0	0	0	2	4	4	0	2
Step[T]Alt	2	2	2	2	2	2	2	2	2	2	2	3
Step[T][S]	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][FP]	2	2	3	2	2	2	2	2	2	2	2	2
Step[T][S][HP]	2	2	2	2	2	2	2	2	2	2	2	3
Step[T][S][HP]Async	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][L]	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][L]Cache	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S]Sparse	2	2	2	2	2	2	2	2	2	2	2	2
[T]Alt	0	6	0	0	0	0	0	5	6	3	0	5
[T][S]	0	4	0	0	0	0	0	4	4	4	0	5
[T][S][FP]	0	4	0	0	0	0	0	2	5	2	0	2
[T][S][HP]	0	3	0	0	0	0	0	2	4	2	0	2
[T][S][HP]Async	0	4	0	0	0	0	0	2	3	2	0	2
[T][S][L]	0	5	0	0	0	0	0	2	5	5	0	2
[T][S][L]Cache	0	5	0	0	0	0	0	2	5	3	0	2
[T][S]Sparse	0	4	0	0	0	0	0	2	4	4	0	2
sgd	5	4	4	0	5	5	5	2	2	5	6	5
step_sgd	0	4	0	0	0	0	0	2	3	2	0	2
step_tween	2	2	2	2	2	2	2	2	2	2	2	2
step_tween_chain	0	3	0	0	0	0	0	2	4	2	0	2
tween	2	2	2	2	2	2	2	2	2	2	2	2
tween_chain	6	1	5	0	5	6	6	2	4	6	6	6

Honesty - mean SoftAcc, every mode x dtype (cols 13-24)

Honesty - mean SoftAcc, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	1	4	5	4	3	4	5	6	5	4	4	4
Mesh[T]	2	2	2	2	2	2	2	2	2	2	2	2
Mesh[T]Alt	6	5	6	6	6	6	6	5	6	5	6	6
Mesh[T]Chain	3	5	4	3	4	2	5	5	4	4	4	3
Mesh[T][S]	4	3	4	4	4	4	4	4	4	4	4	4
Mesh[T][S][FP]	3	4	5	3	3	4	4	2	4	4	4	4
Mesh[T][S]Sparse	4	4	4	3	4	3	4	5	3	3	4	3
Step[T]Alt	2	2	2	2	2	2	2	3	2	2	2	2
Step[T][S]	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][FP]	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][HP]	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][HP]Async	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][L]	2	2	2	2	2	2	2	3	2	2	2	2
Step[T][S][L]Cache	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S]Sparse	2	2	2	2	2	2	2	2	2	2	2	2
[T]Alt	6	5	6	6	6	6	6	5	5	6	5	6
[T][S]	4	4	4	4	4	4	4	5	4	4	4	4
[T][S][FP]	4	5	4	4	4	4	4	2	4	2	2	4
[T][S][HP]	4	5	2	3	4	4	4	2	4	4	4	3
[T][S][HP]Async	1	5	3	3	4	5	3	2	3	4	3	3
[T][S][L]	4	5	5	4	5	5	4	2	4	5	4	5
[T][S][L]Cache	5	5	5	5	5	5	5	2	5	5	5	5
[T][S]Sparse	4	4	4	4	4	4	4	2	4	4	3	4
sgd	4	5	4	4	2	4	5	5	4	4	4	4
step_sgd	4	4	4	3	4	4	4	2	4	3	2	4
step_tween	2	2	2	2	2	2	2	2	2	2	2	2
step_tween_chain	4	4	4	4	4	4	4	2	3	3	3	4
tween	2	2	2	2	2	2	2	2	2	2	2	2
tween_chain	3	5	4	4	4	4	4	5	4	1	4	4

Honesty - mean SoftAcc, every mode x dtype (cols 25-34)

Honesty - mean SoftAcc, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	4	4	4	4	4	4	4	4	4	2
Mesh[T]	2	2	2	2	2	2	2	2	2	2
Mesh[T]Alt	5	5	6	6	6	6	5	6	6	6
Mesh[T]Chain	1	4	4	4	5	4	4	4	4	3
Mesh[T][S]	4	4	4	4	4	4	4	4	4	4
Mesh[T][S][FP]	4	5	4	4	4	3	3	4	5	3
Mesh[T][S]Sparse	4	3	3	3	3	4	4	3	3	3
Step[T]Alt	2	2	2	2	2	2	2	2	2	2
Step[T][S]	2	2	2	2	2	2	2	2	2	2
Step[T][S][FP]	2	2	2	2	2	2	2	2	2	2
Step[T][S][HP]	2	2	2	2	2	2	2	2	2	2
Step[T][S][HP]Async	2	2	2	2	2	2	2	2	2	2
Step[T][S][L]	2	2	2	2	2	2	2	2	2	2
Step[T][S][L]Cache	2	2	2	2	2	2	2	2	2	2
Step[T][S]Sparse	2	2	2	2	2	2	2	2	2	2
[T]Alt	6	6	6	6	6	6	6	6	6	5
[T][S]	4	4	4	4	4	4	4	4	4	4
[T][S][FP]	4	4	3	4	3	4	3	4	4	4
[T][S][HP]	4	4	5	3	3	4	5	3	4	4
[T][S][HP]Async	3	3	4	3	3	3	3	3	3	3
[T][S][L]	4	4	5	5	5	4	4	4	4	5
[T][S][L]Cache	5	5	5	5	4	5	5	5	5	5
[T][S]Sparse	3	3	4	4	3	4	4	4	4	3
sgd	4	4	4	4	4	4	5	1	4	1
step_sgd	4	4	4	3	4	4	4	4	4	3
step_tween	2	2	2	2	2	2	2	2	2	2
step_tween_chain	4	5	4	4	4	4	4	4	4	3
tween	2	2	2	2	2	2	2	2	2	2
tween_chain	4	1	4	1	4	4	4	4	4	4

Honesty - mean Avail, every mode x dtype (cols 1-12)

Honesty - mean Avail, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	22	21	23	23	23	23	24	21	24	23	23	23
Mesh[T]	20	18	21	21	21	20	21	19	21	21	20	21
Mesh[T]Alt	23	13	23	23	23	23	23	14	16	17	23	16
Mesh[T]Chain	22	21	24	24	23	23	23	22	24	23	23	23
Mesh[T][S]	27	25	28	28	27	26	27	26	29	28	27	29
Mesh[T][S][FP]	26	24	29	29	27	26	27	27	29	28	27	28
Mesh[T][S]Sparse	36	36	36	36	36	36	36	36	37	36	36	37
Step[T]Alt	16	14	18	17	16	17	17	15	17	17	16	17
Step[T][S]	23	22	25	25	24	23	24	23	25	24	24	25
Step[T][S][FP]	23	21	24	24	24	22	24	22	25	24	24	25
Step[T][S][HP]	23	20	24	24	23	23	24	22	24	24	22	24
Step[T][S][HP]Async	23	21	25	25	24	23	24	22	24	25	23	24
Step[T][S][L]	30	29	30	31	30	30	30	29	30	30	30	30
Step[T][S][L]Cache	30	30	31	30	31	30	30	29	30	30	30	30
Step[T][S]Sparse	24	21	24	25	24	22	24	22	24	24	24	25
[T]Alt	23	13	23	23	23	23	23	14	16	17	23	17
[T][S]	26	25	28	28	27	27	27	25	29	28	28	29
[T][S][FP]	26	24	28	28	27	26	28	26	29	28	28	28
[T][S][HP]	26	24	29	28	27	26	27	26	29	28	27	29
[T][S][HP]Async	26	24	29	28	27	26	27	26	29	28	27	28
[T][S][L]	35	33	36	36	35	36	36	36	35	35	36	37
[T][S][L]Cache	35	36	36	36	35	36	36	36	37	37	35	37
[T][S]Sparse	36	36	36	37	36	36	36	35	37	36	36	36
sgd	23	21	24	24	23	23	24	23	24	24	23	24
step_sgd	26	24	27	27	27	26	28	26	28	27	28	28
step_tween	23	20	24	23	23	22	24	22	23	24	23	24
step_tween_chain	25	24	27	27	26	26	27	25	27	27	27	28
tween	20	18	21	21	21	21	21	20	21	21	21	20
tween_chain	23	21	24	24	23	23	23	22	24	23	23	24

Honesty - mean Avail, every mode x dtype (cols 13-24)

Honesty - mean Avail, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	24	21	23	24	21	24	24	24	22	24	21	23
Mesh[T]	21	18	21	21	19	21	21	21	20	20	18	20
Mesh[T]Alt	16	13	16	16	14	16	16	16	14	15	13	15
Mesh[T]Chain	23	20	24	24	21	24	24	24	22	23	21	23
Mesh[T][S]	28	24	29	28	24	29	29	28	26	28	25	28
Mesh[T][S][FP]	28	24	29	28	25	29	29	28	26	29	25	28
Mesh[T][S]Sparse	36	35	37	36	36	37	37	36	35	36	35	37
Step[T]Alt	17	14	17	17	15	17	17	18	16	17	13	17
Step[T][S]	24	21	24	24	22	25	25	24	23	24	21	24
Step[T][S][FP]	24	21	24	24	21	25	25	24	22	24	21	24
Step[T][S][HP]	24	21	24	24	20	24	24	24	22	24	19	23
Step[T][S][HP]Async	25	21	25	24	21	25	24	24	22	24	21	23
Step[T][S][L]	30	28	30	31	30	29	30	30	29	29	29	30
Step[T][S][L]Cache	30	29	29	30	30	30	30	31	29	29	29	31
Step[T][S]Sparse	25	21	24	24	21	24	24	25	22	24	21	24
[T]Alt	16	13	16	16	13	16	16	16	14	16	13	15
[T][S]	28	24	29	29	25	29	29	28	26	28	24	28
[T][S][FP]	28	24	29	28	25	29	29	28	26	28	25	28
[T][S][HP]	29	24	29	28	25	29	29	29	26	28	24	28
[T][S][HP]Async	29	24	29	28	24	29	29	28	26	28	25	28
[T][S][L]	36	33	36	36	34	35	35	37	34	35	34	35
[T][S][L]Cache	37	35	37	37	36	37	37	37	36	36	36	37
[T][S]Sparse	36	35	37	36	35	36	37	36	36	36	35	37
sgd	25	21	24	24	22	25	24	24	23	24	21	24
step_sgd	28	23	28	28	24	28	28	28	26	27	23	28
step_tween	24	20	23	24	21	23	24	24	22	24	19	23
step_tween_chain	27	23	27	27	23	27	27	27	25	27	23	27
tween	21	18	21	21	18	21	21	21	20	21	17	21
tween_chain	23	20	23	24	21	24	24	23	22	24	21	23

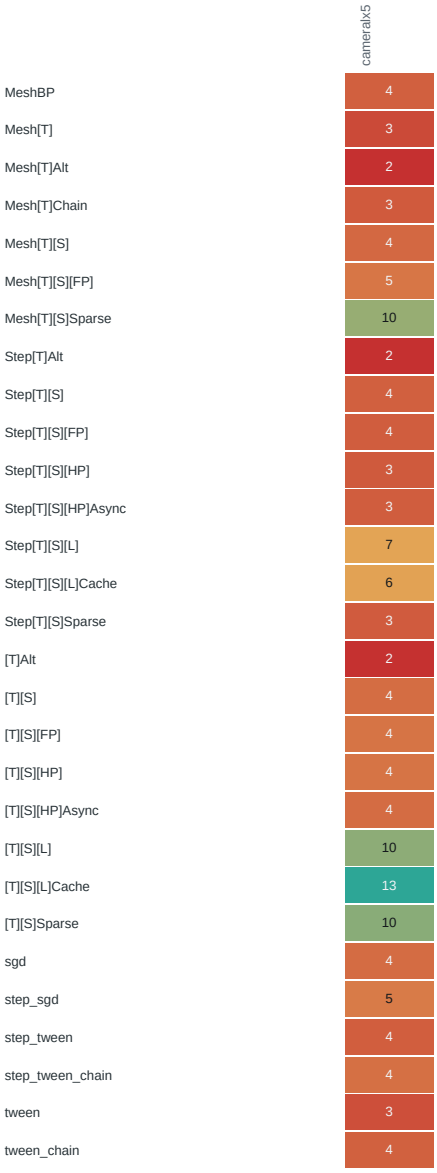
Honesty - mean Avail, every mode x dtype (cols 25-34)

Honesty - mean Avail, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	23	23	23	23	23	23	24	23	23	23
Mesh[T]	20	20	21	21	20	21	21	21	20	21
Mesh[T]Alt	15	15	15	15	15	16	16	15	15	15
Mesh[T]Chain	23	22	23	23	23	24	23	23	23	24
Mesh[T][S]	28	27	28	28	28	29	29	28	26	28
Mesh[T][S][FP]	28	28	28	28	27	29	29	28	27	28
Mesh[T][S]Sparse	36	36	36	37	36	37	37	36	36	37
Step[T]Alt	17	17	17	17	16	17	17	17	16	17
Step[T][S]	24	23	24	24	24	24	24	24	23	24
Step[T][S][FP]	23	24	24	24	24	24	24	24	23	24
Step[T][S][HP]	23	23	23	24	23	23	23	23	23	24
Step[T][S][HP]Async	24	23	24	24	24	24	24	24	23	24
Step[T][S][L]	30	29	30	30	31	30	30	30	30	31
Step[T][S][L]Cache	30	30	30	30	30	30	30	30	29	30
Step[T][S]Sparse	24	24	24	24	24	25	25	23	23	24
[T]Alt	15	15	15	16	15	16	16	15	15	15
[T][S]	27	27	29	27	27	29	29	27	27	28
[T][S][FP]	28	28	28	28	28	29	29	28	27	28
[T][S][HP]	28	28	29	27	27	29	29	28	27	28
[T][S][HP]Async	28	28	28	28	28	29	29	27	26	27
[T][S][L]	36	36	34	36	36	35	35	36	34	35
[T][S][L]Cache	37	37	37	37	37	37	37	37	37	37
[T][S]Sparse	37	36	37	36	36	36	37	36	36	37
sgd	24	24	24	24	24	24	24	24	24	24
step_sgd	28	27	27	28	27	27	28	28	27	27
step_tween	23	23	24	23	23	24	24	23	23	23
step_tween_chain	26	27	27	27	27	27	27	27	26	27
tween	21	21	21	21	21	21	21	21	21	21
tween_chain	23	23	24	23	24	24	24	23	23	23

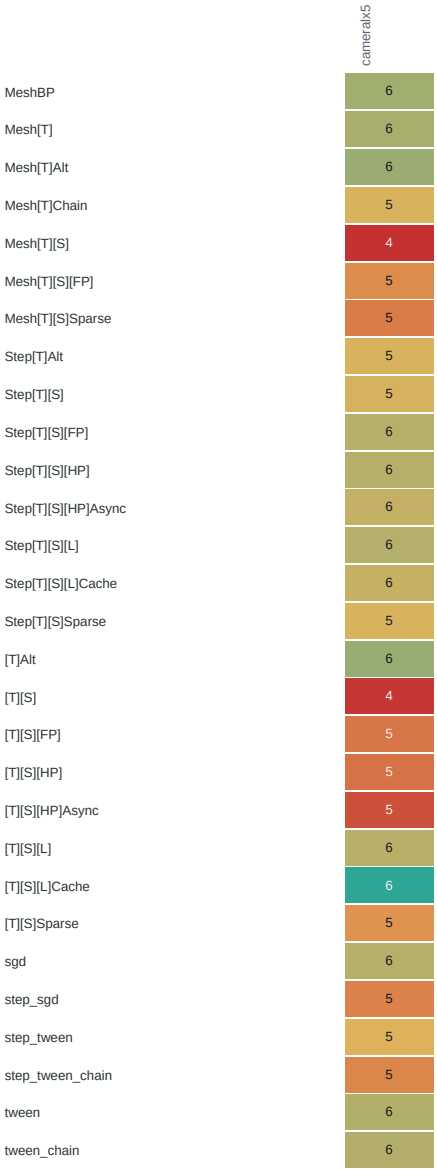
Mean Score, every mode x arch

Mean Score, every mode x arch



Mean hard Acc, every mode x arch

Mean hard Acc, every mode x arch

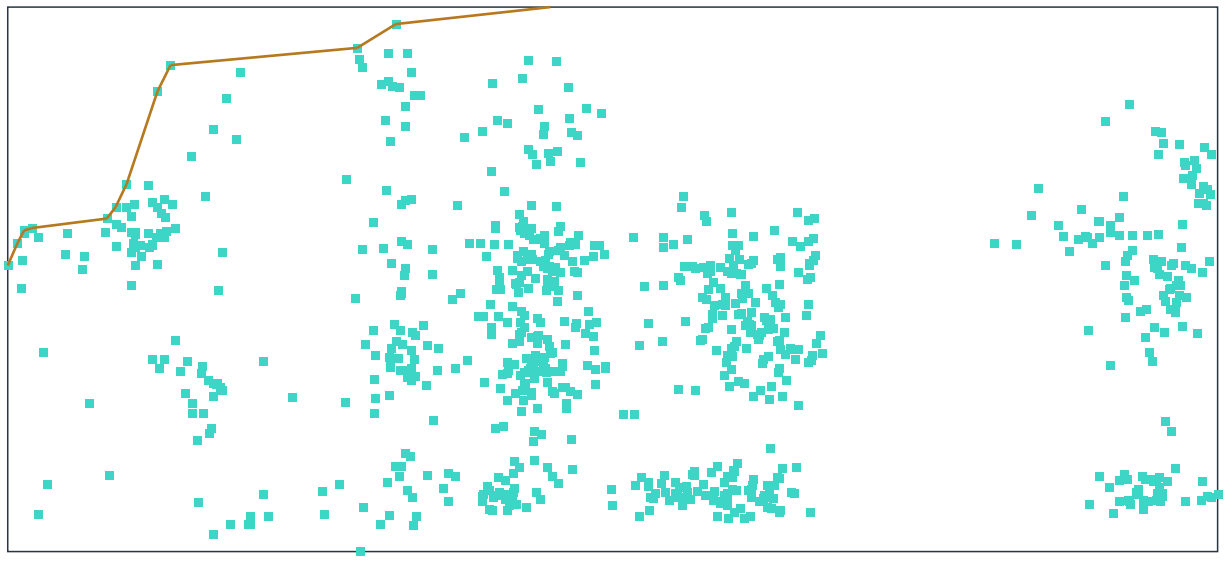


Mean Avail, every mode x arch

Mean Avail, every mode x arch

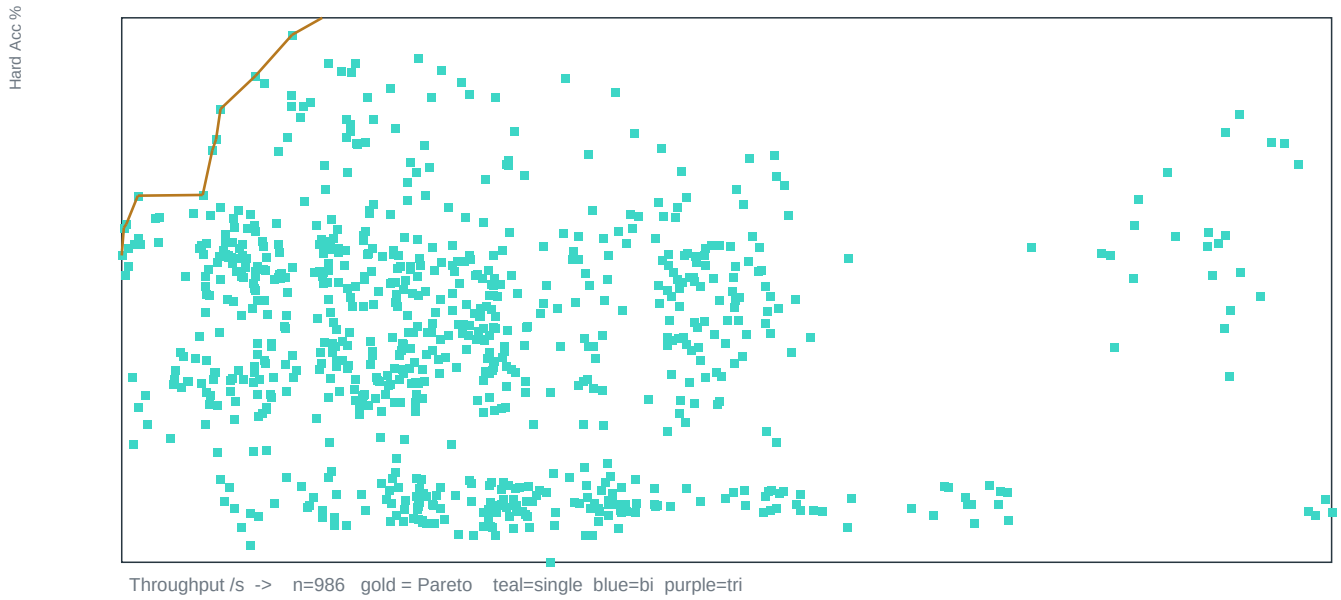
	cameralx5
MeshBP	23
Mesh[T]	20
Mesh[T]Alt	17
Mesh[T]Chain	23
Mesh[T][S]	27
Mesh[T][S][FP]	28
Mesh[T][S]Sparse	36
Step[T]Alt	16
Step[T][S]	24
Step[T][S][FP]	23
Step[T][S][HP]	23
Step[T][S][HP]Async	24
Step[T][S][L]	30
Step[T][S][L]Cache	30
Step[T][S]Sparse	24
[T]Alt	17
[T][S]	27
[T][S][FP]	28
[T][S][HP]	28
[T][S][HP]Async	27
[T][S][L]	35
[T][S][L]Cache	37
[T][S]Sparse	36
sgd	24
step_sgd	27
step_tween	23
step_tween_chain	26
tween	20
tween_chain	23

Pillars - Availability vs hard Acc

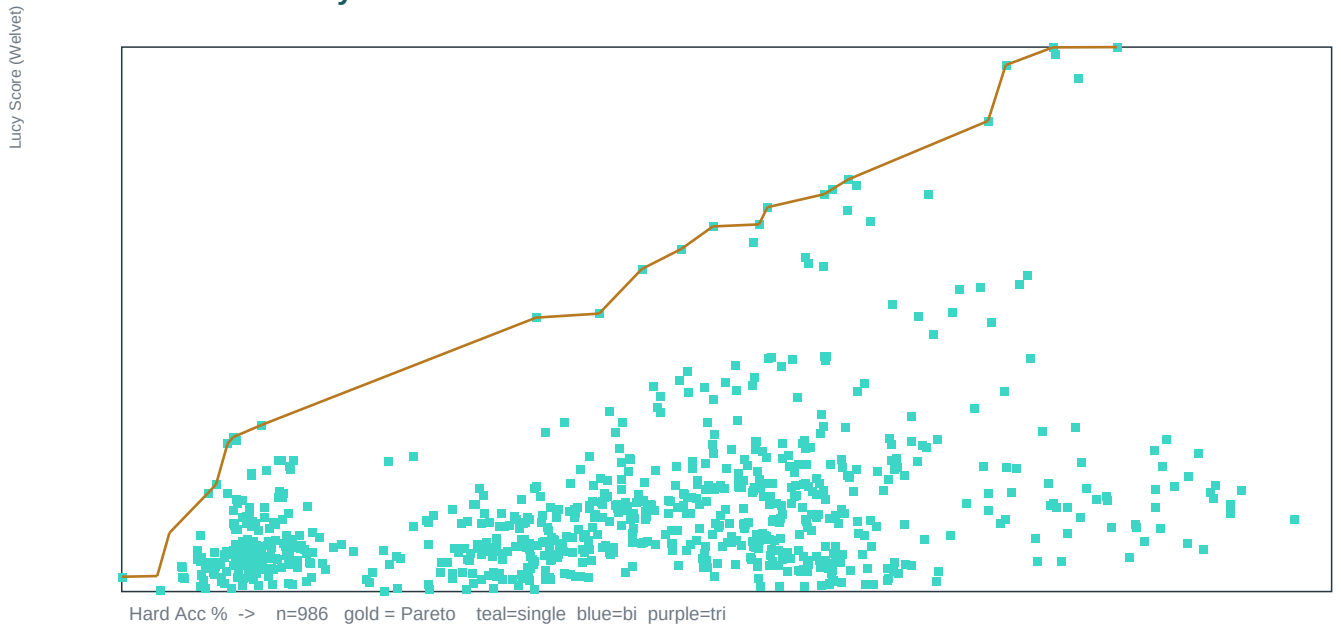



Availability % -> n=986 gold = Pareto teal=single blue=bi purple=tri
Hard Acc %

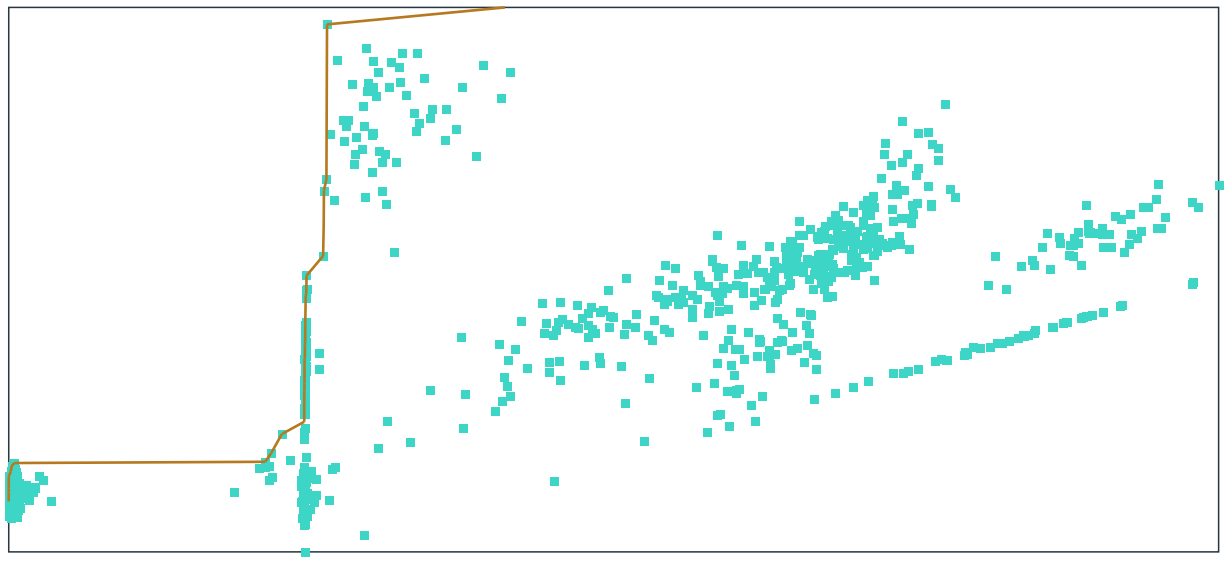
Pillars - Throughput vs hard Acc



Pareto - hard Acc vs Lucy Score

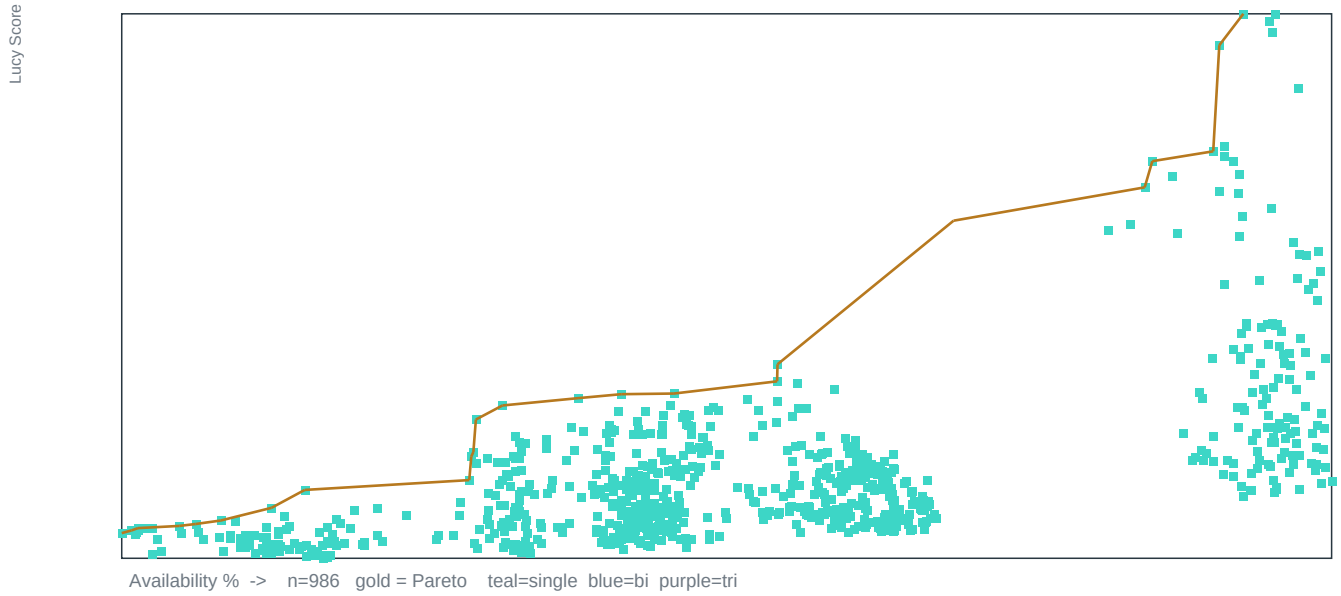


SoftAcc (serve-confidence) vs hard Acc

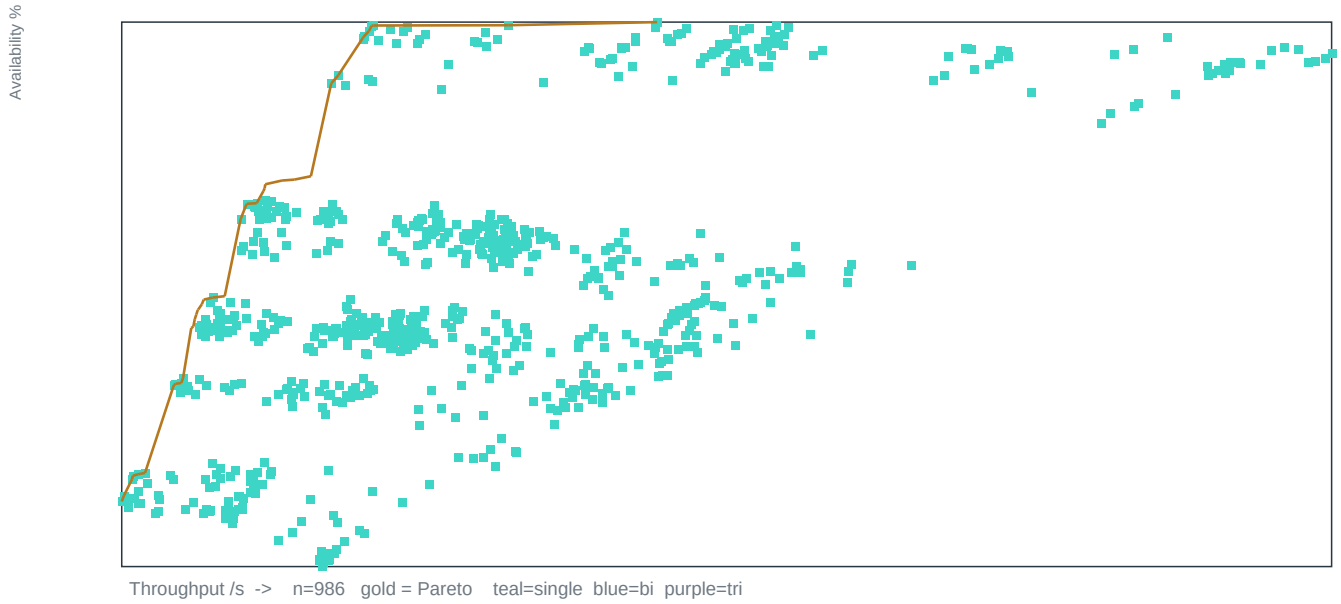



SoftAcc % -> n=986 gold = Pareto teal=single blue=bi purple=tri
Hard Acc %

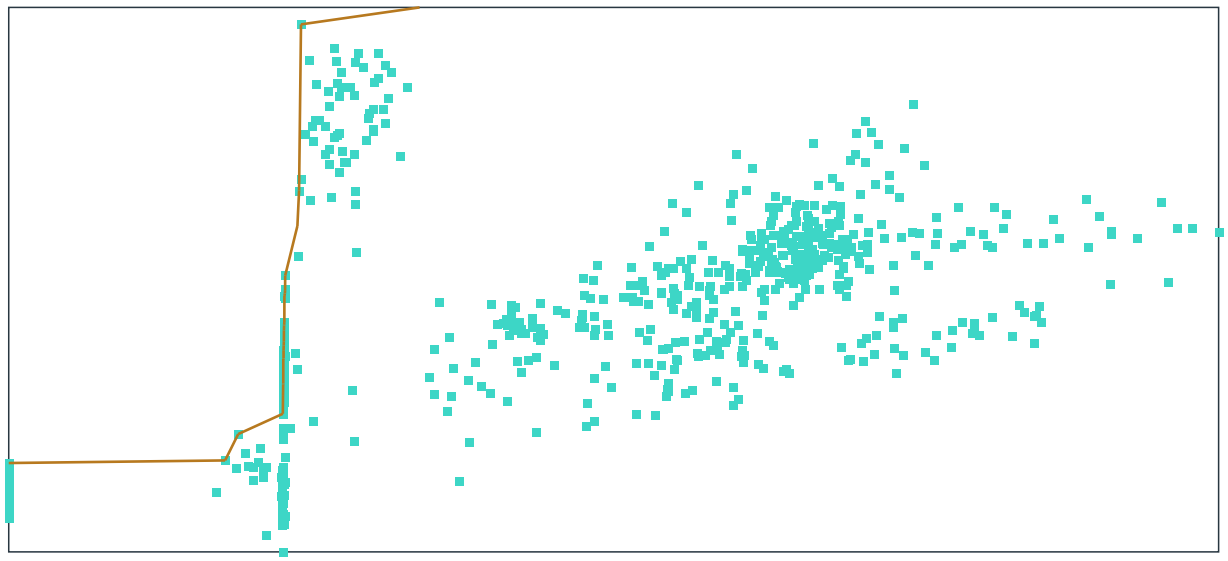
Avail vs Lucy Score (duty clock)



Pillars - Throughput vs Availability



AdaptPct vs hard Acc



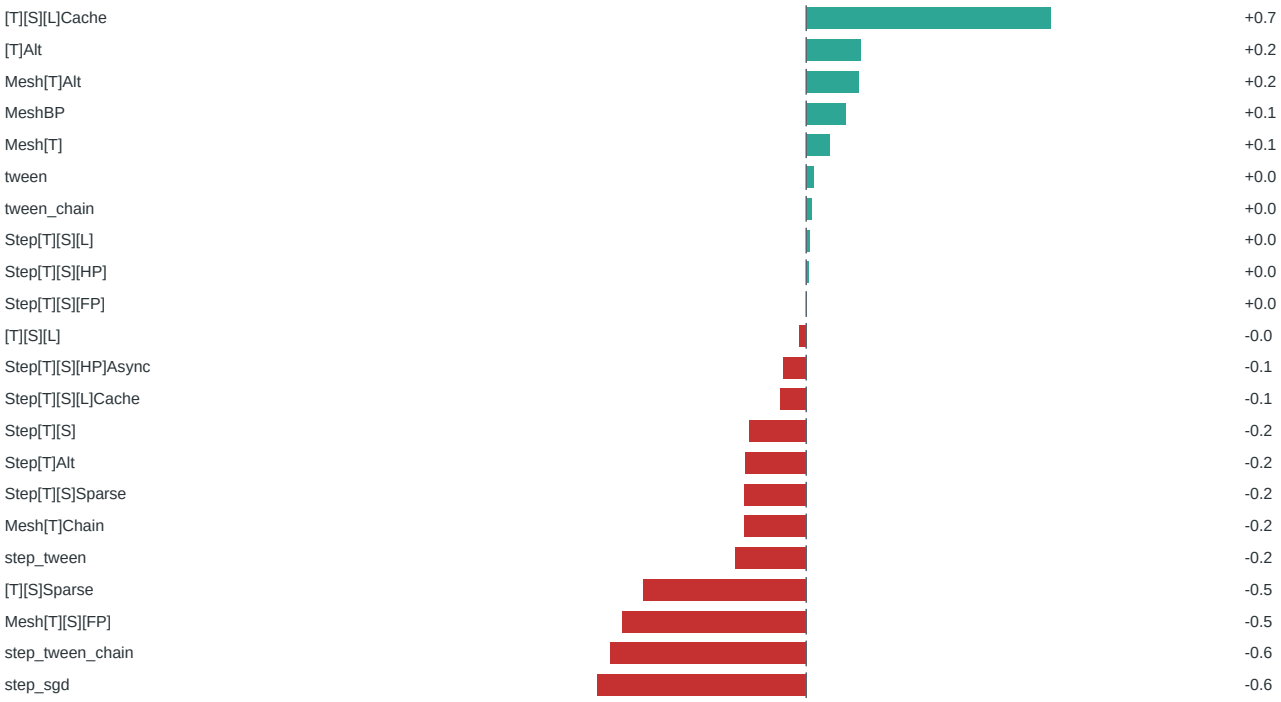

AdaptPct % -> n=986 gold = Pareto teal=single blue=bi purple=tri
Hard Acc %

vs sgd - matched dtype x format x arch

AccDelta is the honest column. ScoreDelta is usually Availability (duty clock), not a better chain rule. Acc win = AccDelta > 0.5. Score win = ScoreDelta > 1. Baseline is discovered from the board, not a frozen StepBP list.

mode	n	AccD	Acc win%	SoftD	AvailD	ThruD	ScoreD	Score win%
[T][S][L]Cache	34	+0.7	65	-0.5	+12.9	+240	+8.7	91
[T]Alt	34	+0.2	44	+0.4	-6.8	-131	-2.6	0
Mesh[T]Alt	34	+0.2	35	+0.4	-6.8	-137	-2.6	0
MeshBP	34	+0.1	26	+0.1	-0.6	-37	-0.5	6
Mesh[T]	34	+0.1	38	-2.3	-3.3	-85	-1.5	6
tween	34	+0.0	41	-2.3	-3.1	-68	-1.3	15
tween_chain	34	+0.0	29	+0.0	-0.6	-28	-0.5	9
Step[T][S][L]	34	+0.0	38	-2.3	+6.4	+77	+2.4	53
Step[T][S][HP]	34	+0.0	38	-2.2	-0.7	-57	-0.8	24
Step[T][S][FP]	34	+0.0	41	-2.3	-0.1	-49	-0.6	26
[T][S][L]	34	-0.0	32	-0.6	+11.6	+206	+5.8	91
Step[T][S][HP]Async	34	-0.1	41	-2.3	-0.1	-50	-0.7	21
Step[T][S][L]Cache	34	-0.1	41	-2.3	+6.4	+74	+2.3	53
Step[T][S]	34	-0.2	41	-2.3	+0.1	-35	-0.5	26
Step[T]Alt	34	-0.2	38	-2.2	-7.1	-146	-2.6	0
Step[T][S]Sparse	34	-0.2	38	-2.3	-0.0	-50	-0.7	21
Mesh[T]Chain	34	-0.2	26	-0.1	-0.7	-42	-0.8	12
step_tween	34	-0.2	38	-2.3	-0.6	-33	-0.6	26
[T][S]Sparse	34	-0.5	15	-1.2	+12.6	+234	+5.9	97
Mesh[T][S][FP]	34	-0.5	24	-1.1	+3.9	+24	+0.4	44
step_tween_chain	34	-0.6	18	-1.2	+2.7	+27	+0.2	24
step_sgd	34	-0.6	18	-1.2	+3.3	+53	+0.6	41
Mesh[T][S]Sparse	34	-0.7	12	-1.3	+12.6	+232	+5.5	100
[T][S][FP]	34	-0.7	15	-1.2	+3.9	+25	+0.3	35
[T][S][HP]	34	-0.7	18	-1.2	+4.0	+28	+0.3	35
[T][S][HP]Async	34	-1.0	18	-1.6	+3.8	+21	-0.0	18
[T][S]	34	-1.2	15	-0.8	+3.8	+36	+0.0	15
Mesh[T][S]	34	-1.2	15	-0.8	+3.8	+22	-0.2	18

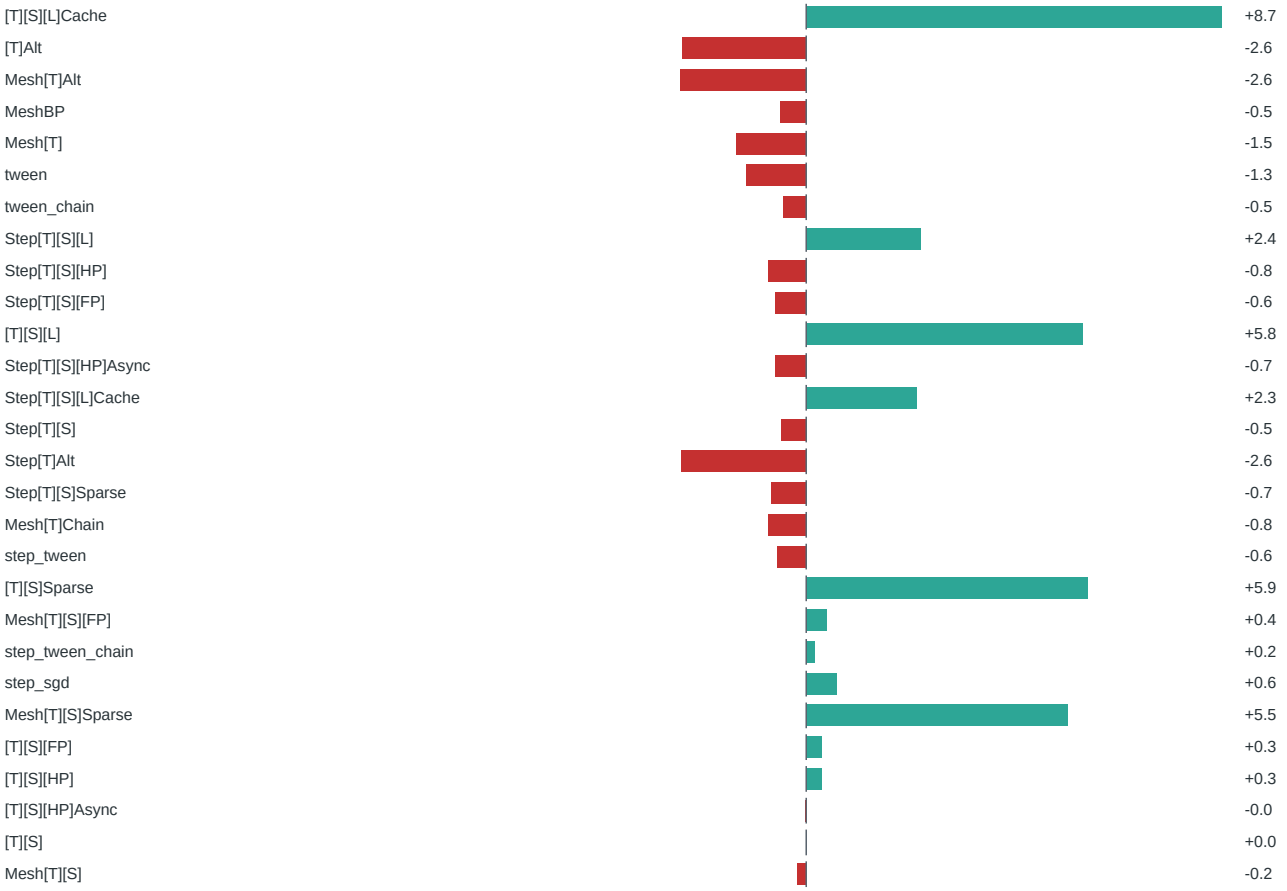
mean AccD vs sgd



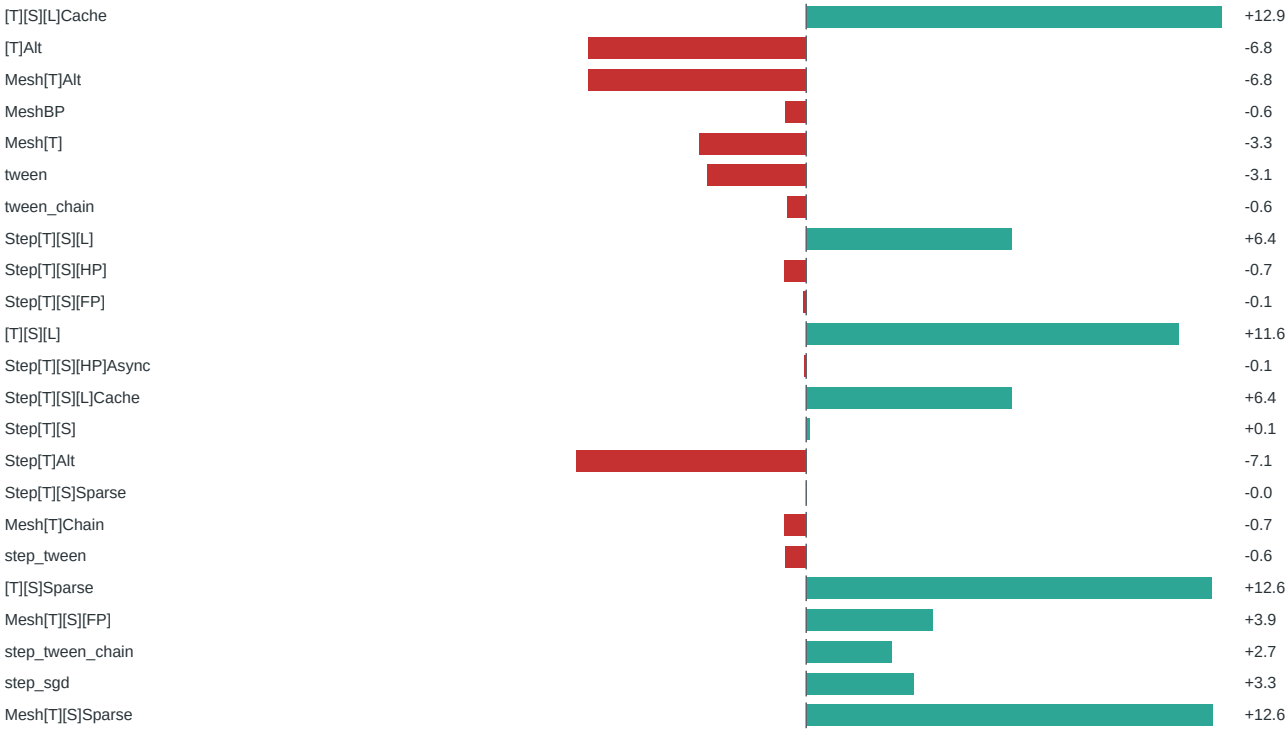
mean AccD vs sgd



mean ScoreD vs sgd (duty clock)



mean AvailD vs sgd



mean AvailD vs sgd



AccD vs sgd, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	-0	+0	+1	+3	-2	-0	-1	+0	+3	-0	-2	+1
Mesh[T]	+5	-4	+5	+6	+4	+4	+4	+0	+2	+5	+2	+4
Mesh[T]Alt	-3	+1	-2	+0	-2	-3	-3	+4	+4	-3	-3	-1
Mesh[T]Chain	+0	-3	+1	+3	+1	-0	+1	-0	+4	-1	-1	-3
Mesh[T][S]	-3	-1	-2	+0	-2	-3	-2	+1	+2	-0	-4	-0
Mesh[T][S][FP]	-3	+0	-2	+1	-2	-3	-2	-0	+3	-2	-4	-2
Mesh[T][S]Sparse	-2	-1	-2	-0	-2	-3	-2	-0	+4	-1	-3	-2
Step[T]Alt	+4	-1	+4	+6	+5	+3	+1	+0	+1	+3	+1	+4
Step[T][S]	+3	-2	+5	+7	+3	+2	+3	-0	+1	+4	+2	+3
Step[T][S][FP]	+3	-2	+6	+6	+5	+3	+4	-0	+2	+2	+3	+3
Step[T][S][HP]	+4	-3	+4	+6	+5	+3	+4	+0	+1	+3	+3	+6
Step[T][S][HP]Async	+3	-1	+5	+6	+4	+3	+4	+0	+1	+3	+1	+4
Step[T][S][L]	+2	-2	+4	+6	+4	+3	+3	-0	+2	+4	+2	+5
Step[T][S][L]Cache	+3	-2	+5	+6	+3	+4	+4	+0	+2	+3	+1	+4
Step[T][S]Sparse	+5	-2	+5	+6	+3	+3	+2	-0	+2	+2	+2	+4
[T]Alt	-3	+1	-2	-0	-3	-3	-3	+4	+3	-2	-4	-0
[T][S]	-3	-1	-2	+0	-2	-3	-3	+1	+1	-1	-4	+0
[T][S][FP]	-3	+0	-2	+0	-2	-3	-3	-0	+4	-3	-3	-2
[T][S][HP]	-3	-1	-2	-0	-2	-3	-2	+0	+4	-3	-4	-2
[T][S][HP]Async	-3	-0	-2	+0	-2	-3	-3	-0	+2	-2	-4	-2
[T][S][L]	-3	+1	-2	+0	-2	-3	-3	+0	+4	+0	-4	-2
[T][S][L]Cache	-2	+3	-2	+0	-2	-3	-3	-0	+4	-2	-3	-2
[T][S]Sparse	-2	+0	-2	+1	-2	-3	-3	-0	+4	-1	-3	-2
step_sgd	-3	+0	-2	+0	-2	-3	-3	+0	+2	-3	-3	-3
step_tween	+4	-5	+5	+7	+3	+3	+3	+0	+2	+4	+0	+4
step_tween_chain	-3	-2	-2	+0	-2	-3	-3	-0	+3	-2	-4	-3
tween	+5	-4	+5	+7	+5	+4	+4	+0	+2	+3	+1	+5
tween_chain	+0	-3	+1	+0	+0	+0	+0	+0	+3	+1	-0	+1

AccD vs sgd, every mode x dtype (cols 13-24)

AccD vs sgd, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	-4	+0	+1	-0	+1	-0	+0	+0	+1	+0	-0	-0
Mesh[T]	-2	-5	-4	-2	+0	-2	-2	+5	-0	-2	-5	-1
Mesh[T]Alt	+0	-1	+1	-0	+3	+0	+0	-1	+1	+0	+0	+1
Mesh[T]Chain	-2	-0	-0	-2	+3	-3	+0	-0	-0	+0	-1	-1
Mesh[T][S]	-2	-3	-1	-2	+1	-1	-2	-1	-1	-2	-2	-1
Mesh[T][S][FP]	-1	-1	+0	-2	+1	-0	-0	-3	+0	+0	+0	+1
Mesh[T][S]Sparse	-1	-0	-1	-1	+2	-1	-0	-0	-1	-1	+0	+0
Step[T]Alt	-1	-5	-3	-2	+0	-2	-2	+4	-1	-2	-4	-2
Step[T][S]	-1	-4	-3	-3	+1	-2	-2	+3	-2	-2	-5	-2
Step[T][S][FP]	-2	-5	-2	-2	+1	-2	-2	+4	-2	-1	-4	-2
Step[T][S][HP]	-2	-5	-2	-2	+0	-2	-2	+4	-1	-2	-5	-1
Step[T][S][HP]Async	-2	-5	-2	-2	+1	-2	-2	+4	-0	-2	-4	-2
Step[T][S][L]	-2	-4	-2	-2	+0	-2	-2	+4	-2	-1	-3	-1
Step[T][S][L]Cache	-2	-5	-2	-2	+1	-2	-2	+4	-1	-2	-5	-1
Step[T][S]Sparse	-3	-5	-2	-2	+1	-2	-2	+4	-2	-2	-4	-2
[T]Alt	+1	-1	+1	-0	+3	+0	+1	-1	+0	+1	-1	+1
[T][S]	-1	-2	-1	-2	+1	-1	-2	-1	-1	-1	-2	-1
[T][S][FP]	-1	-0	-0	-1	+3	+0	+0	-3	+1	-3	-1	-1
[T][S][HP]	-0	-1	-3	-1	+3	+1	-1	-3	+0	-0	+0	-2
[T][S][HP]Async	-4	-1	-1	-1	+3	+1	-2	-2	-1	+1	-1	-1
[T][S][L]	+0	-1	+1	-1	+4	+0	+0	-3	+1	+1	+1	+1
[T][S][L]Cache	+2	+1	+2	+1	+5	+1	+1	-3	+2	+2	+2	+1
[T][S]Sparse	-1	-1	+0	+0	+3	-1	-1	-3	+0	+0	-0	-1
step_sgd	-0	-1	+1	-2	+3	-0	-0	-3	+1	-1	-2	+0
step_tween	-2	-5	-4	-2	+2	-1	-2	+3	-0	-2	-4	-2
step_tween_chain	-0	-0	+1	-2	+3	-1	-0	-2	-1	-1	-3	-0
tween	-1	-5	-4	-3	+1	-1	-2	+5	-2	-3	-5	-1
tween_chain	-2	-1	+1	-1	+3	+0	-1	-0	+1	-3	+0	+1

AccD vs sgd, every mode x dtype (cols 25-34)

AccD vs sgd, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	+0	-0	+0	-0	+0	-1	-0	+3	-0	+1
Mesh[T]	-1	-4	-3	-2	-2	-2	-2	+3	-3	+2
Mesh[T]Alt	+0	+0	+1	+1	+0	+1	-0	+3	-0	+5
Mesh[T]Chain	-3	+0	+1	-1	+0	-1	-1	+3	-0	+1
Mesh[T][S]	-1	-1	-2	-2	-2	-2	-2	+2	-3	+2
Mesh[T][S][FP]	+1	+0	+1	-1	-1	-2	-1	+3	+0	+2
Mesh[T][S]Sparse	+0	-2	-0	-1	-0	+0	-1	+2	-2	+2
Step[T]Alt	-2	-4	-2	-2	-2	-3	-3	+1	-2	+1
Step[T][S]	-2	-4	-1	-2	-2	-3	-3	+1	-3	+2
Step[T][S][FP]	-2	-4	-2	-2	-2	-2	-2	+1	-3	+2
Step[T][S][HP]	-2	-4	-2	-2	-2	-2	-2	+1	-3	+2
Step[T][S][HP]Async	-1	-4	-2	-2	-2	-2	-2	+1	-2	+1
Step[T][S][L]	-1	-4	-1	-2	-2	-2	-3	+1	-3	+2
Step[T][S][L]Cache	-2	-3	-2	-3	-2	-2	-3	+1	-3	+2
Step[T][S]Sparse	-2	-4	-2	-2	-1	-2	-3	+0	-3	+2
[T]Alt	+1	+1	+1	+0	+1	+0	-0	+3	-0	+3
[T][S]	-1	-1	-1	-2	-2	-2	-3	+1	-3	+2
[T][S][FP]	-0	-0	-0	-0	-1	-1	-2	+2	-1	+3
[T][S][HP]	-0	+0	+1	-2	-1	-0	-0	+1	-1	+3
[T][S][HP]Async	-2	-1	+0	-1	-1	-1	-2	+2	-1	+3
[T][S][L]	-0	-0	+1	-0	+0	+0	-0	+3	-1	+4
[T][S][L]Cache	+2	+1	+2	+1	+1	+1	+0	+4	+1	+5
[T][S]Sparse	-0	-1	-0	-0	-1	-0	-1	+3	-1	+3
step_sgd	-0	-0	+0	-1	-0	-1	-0	+3	-1	+3
step_tween	-2	-4	-4	-2	-2	-2	-2	+1	-1	+1
step_tween_chain	+0	+1	+0	+0	-0	-0	-1	+3	-1	+2
tween	-0	-4	-4	-2	-2	-2	-2	+2	-2	+2
tween_chain	-0	-3	+0	-4	+0	-0	-0	+3	-0	+4

ScoreD vs sgd, every mode x dtype (cols 1-12)

ScoreD vs sgd, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	-1	-1	+0	+1	-2	-1	-1	-0	+1	-1	-2	-0
Mesh[T]	+1	-5	+1	+2	+1	+0	+1	-1	+0	+1	-1	+1
Mesh[T]Alt	-3	-4	-2	-0	-2	-5	-3	-1	-0	-3	-3	-2
Mesh[T]Chain	-1	-4	+0	+1	-0	-2	-1	-1	+1	-1	-1	-2
Mesh[T][S]	-2	+0	-1	+1	-1	-3	-2	+2	+1	+1	-2	+1
Mesh[T][S][FP]	-2	+1	-1	+1	-1	-3	-2	+0	+2	-1	-2	-1
Mesh[T][S]Sparse	+2	+11	+1	+2	+1	+1	+2	+4	+5	+4	+1	+1
Step[T]Alt	-2	-5	-1	+1	-1	-3	-3	-2	-1	-2	-2	-1
Step[T][S]	+2	-2	+3	+4	+2	+1	+2	-0	+0	+1	+1	+2
Step[T][S][FP]	+2	-3	+3	+3	+2	+1	+3	-1	+0	+1	+1	+1
Step[T][S][HP]	+2	-4	+1	+3	+2	+2	+3	-0	+0	+1	+0	+3
Step[T][S][HP]Async	+1	-2	+2	+3	+2	+1	+2	-0	+0	+1	-0	+1
Step[T][S][L]	+6	+2	+5	+7	+6	+9	+8	+1	+2	+5	+5	+6
Step[T][S][L]Cache	+8	+2	+6	+6	+6	+11	+8	+2	+1	+4	+4	+6
Step[T][S]Sparse	+3	-3	+2	+3	+1	+1	+1	-1	+0	+0	+1	+2
[T]Alt	-3	-4	-1	-0	-2	-4	-3	-1	-0	-3	-3	-2
[T][S]	-2	+1	-0	+1	-1	-3	-2	+2	+1	+1	-2	+1
[T][S][FP]	-2	+1	-1	+1	-1	-3	-2	+0	+2	-2	-2	-1
[T][S][HP]	-2	+0	-1	+0	-1	-3	-2	+1	+2	-1	-2	-1
[T][S][HP]Async	-2	+1	-1	+1	-1	-3	-3	+0	+1	-1	-2	-1
[T][S][L]	+1	+12	+1	+3	+2	+2	+1	+5	+5	+5	+0	+1
[T][S][L]Cache	+2	+23	+2	+3	+1	+1	+2	+4	+6	+2	+0	+1
[T][S]Sparse	+2	+14	+1	+3	+1	+1	+1	+3	+5	+4	+1	+2
step_sgd	-2	+2	-1	+1	-1	-3	-1	+1	+1	-1	-1	-1
step_tween	+2	-5	+3	+4	+1	+2	+2	-0	+0	+1	-0	+2
step_tween_chain	-2	-1	-1	+1	-1	-4	-2	+0	+2	-1	-2	-1
tween	+1	-5	+1	+3	+1	+1	+1	-1	+0	-0	-0	+1
tween_chain	-0	-3	+0	+0	-0	-1	-0	-0	+1	+0	-1	+0

ScoreD vs sgd, every mode x dtype (cols 13-24)

ScoreD vs sgd, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	-3	-0	-0	-1	+0	-0	-0	-0	+0	-0	-1	-1
Mesh[T]	-3	-5	-2	-3	-1	-1	-1	+0	-3	-2	-5	-2
Mesh[T]Alt	-3	-5	-2	-4	-2	-2	-2	-3	-5	-2	-5	-3
Mesh[T]Chain	-2	-1	-0	-2	+2	-1	-0	-1	-2	-0	-2	-1
Mesh[T][S]	-1	-2	+0	-0	+2	+0	+0	-0	-0	-0	-1	+1
Mesh[T][S][FP]	-0	+1	+2	-0	+2	+1	+1	-2	+1	+2	+2	+2
Mesh[T][S]Sparse	+6	+15	+4	+6	+14	+3	+4	+5	+8	+4	+15	+7
Step[T]Alt	-3	-6	-2	-4	-2	-2	-2	-1	-5	-3	-6	-3
Step[T][S]	-2	-4	-1	-2	+1	-1	-1	+2	-3	-1	-5	-1
Step[T][S][FP]	-2	-5	-1	-2	+0	-1	-1	+2	-3	-1	-4	-2
Step[T][S][HP]	-2	-5	-1	-2	-1	-1	-1	+1	-3	-1	-5	-2
Step[T][S][HP]Async	-2	-5	-1	-2	+0	-1	-1	+2	-2	-1	-4	-2
Step[T][S][L]	-0	-1	+0	+1	+4	+0	+0	+7	+0	+1	-0	+1
Step[T][S][L]Cache	-0	-2	+0	+0	+6	+0	-0	+7	+2	+0	-3	+1
Step[T][S]Sparse	-2	-5	-1	-2	-0	-1	-1	+2	-3	-1	-5	-2
[T]Alt	-3	-5	-2	-4	-2	-2	-1	-3	-5	-2	-5	-2
[T][S]	-0	-1	+0	-0	+2	+0	+0	+1	+0	+1	-2	+0
[T][S][FP]	-0	+2	+1	+0	+4	+1	+1	-2	+3	-1	-0	+1
[T][S][HP]	+1	+1	-1	-0	+4	+1	+1	-1	+2	+1	+1	+0
[T][S][HP]Async	-2	+0	+1	-0	+4	+1	+0	-2	+0	+1	+0	+0
[T][S][L]	+7	+11	+5	+6	+17	+3	+3	+1	+13	+6	+13	+7
[T][S][L]Cache	+11	+20	+7	+10	+25	+5	+5	+1	+21	+9	+22	+10
[T][S]Sparse	+5	+14	+5	+7	+18	+3	+3	+1	+12	+6	+13	+6
step_sgd	+1	+0	+1	+0	+5	+1	+1	-1	+3	+0	-2	+2
step_tween	-2	-5	-2	-2	+1	-1	-1	+2	-1	-2	-5	-1
step_tween_chain	+1	+1	+1	-0	+4	+0	+0	-2	+0	+0	-2	+1
tween	-2	-5	-2	-3	-1	-1	-1	+1	-3	-2	-5	-2
tween_chain	-2	-1	-0	-1	+2	-0	-0	-1	-0	-2	-1	+0

ScoreD vs sgd, every mode x dtype (cols 25-34)

ScoreD vs sgd, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	-1	-0	-0	-1	-1	-1	-0	+2	-1	+0
Mesh[T]	-2	-3	-2	-3	-3	-1	-1	+1	-5	-0
Mesh[T]Alt	-3	-3	-2	-3	-3	-2	-2	-1	-6	-0
Mesh[T]Chain	-3	-1	+0	-1	-0	-0	-1	+2	-2	+1
Mesh[T][S]	-0	+0	-0	-0	-1	+0	-0	+2	-3	+2
Mesh[T][S][FP]	+2	+2	+2	+1	+0	-0	+1	+3	+1	+3
Mesh[T][S]Sparse	+8	+4	+4	+6	+6	+4	+3	+9	+7	+7
Step[T]Alt	-3	-4	-2	-4	-4	-2	-2	-1	-6	-1
Step[T][S]	-2	-3	-1	-2	-2	-1	-1	+1	-4	+1
Step[T][S][FP]	-2	-3	-1	-2	-2	-1	-1	+0	-4	+1
Step[T][S][HP]	-2	-3	-1	-2	-2	-1	-1	+0	-4	+1
Step[T][S][HP]Async	-2	-3	-1	-2	-2	-1	-1	+0	-4	+0
Step[T][S][L]	+2	-2	+1	+0	+0	+0	-0	+3	+1	+4
Step[T][S][L]Cache	+1	-1	+0	-1	+1	+1	-0	+3	-1	+3
Step[T][S]Sparse	-2	-3	-1	-2	-2	-1	-1	-0	-4	+1
[T]Alt	-3	-3	-2	-3	-3	-2	-2	-1	-6	-1
[T][S]	+0	+0	+0	-0	-0	+0	-0	+2	-2	+3
[T][S][FP]	+1	+1	+1	+1	+0	+0	+0	+3	+0	+4
[T][S][HP]	+1	+2	+2	-1	+0	+1	+1	+1	+0	+3
[T][S][HP]Async	-1	+1	+1	+0	-0	-0	+0	+3	-0	+2
[T][S][L]	+6	+6	+4	+7	+8	+3	+3	+10	+9	+9
[T][S][L]Cache	+12	+11	+8	+11	+10	+6	+5	+14	+17	+13
[T][S]Sparse	+7	+5	+5	+7	+6	+4	+4	+10	+11	+9
step_sgd	+1	+1	+1	+1	+1	+0	+1	+4	+1	+3
step_tween	-2	-3	-2	-2	-2	-1	-1	+1	-2	+1
step_tween_chain	+1	+2	+1	+2	+1	+0	+0	+4	+1	+2
tween	-2	-3	-2	-2	-3	-1	-1	+0	-4	+0
tween_chain	-1	-3	+0	-3	-0	-0	-0	+1	-1	+2

AvailD vs sgd, every mode x dtype (cols 1-12)

AvailD vs sgd, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	-1	-1	-1	-0	-1	-1	+0	-2	-0	-1	-0	-1
Mesh[T]	-3	-4	-3	-3	-3	-3	-3	-4	-3	-3	-4	-3
Mesh[T]Alt	-1	-8	-1	-1	-1	-1	-1	-9	-8	-7	-0	-7
Mesh[T]Chain	-1	-1	-1	-0	-0	-1	-1	-1	-1	-1	-0	-0
Mesh[T][S]	+3	+3	+4	+5	+4	+2	+4	+2	+5	+4	+4	+5
Mesh[T][S][FP]	+3	+3	+5	+5	+4	+3	+3	+4	+5	+4	+4	+5
Mesh[T][S]Sparse	+13	+14	+12	+13	+12	+13	+12	+13	+13	+12	+13	+13
Step[T]Alt	-7	-8	-7	-7	-7	-7	-6	-8	-7	-7	-7	-7
Step[T][S]	+0	+0	+1	+1	+0	-0	+0	-1	+0	+0	+1	+1
Step[T][S][FP]	+0	-0	+0	+0	+0	-1	+0	-1	+0	+0	+1	+1
Step[T][S][HP]	-1	-2	-0	-0	-0	-0	+1	-1	-1	-0	-1	-0
Step[T][S][HP]Async	-0	-0	+1	+1	+0	-0	+0	-1	-0	+1	-0	-0
Step[T][S][L]	+7	+8	+6	+7	+7	+6	+7	+6	+6	+6	+7	+6
Step[T][S][L]Cache	+7	+8	+6	+7	+7	+6	+7	+6	+6	+6	+7	+6
Step[T][S]Sparse	+0	-0	+0	+1	+0	-1	+0	-2	+0	+0	+0	+1
[T]Alt	-0	-8	-2	-1	-0	-1	-1	-9	-8	-7	-1	-7
[T][S]	+3	+3	+4	+5	+3	+3	+4	+2	+5	+4	+4	+5
[T][S][FP]	+3	+3	+4	+5	+4	+3	+4	+3	+5	+4	+4	+4
[T][S][HP]	+3	+3	+4	+5	+4	+3	+4	+3	+5	+4	+4	+5
[T][S][HP]Async	+3	+3	+4	+5	+3	+3	+4	+3	+5	+4	+4	+4
[T][S][L]	+12	+12	+11	+12	+12	+12	+13	+12	+10	+11	+13	+13
[T][S][L]Cache	+12	+14	+11	+12	+12	+12	+13	+13	+13	+13	+12	+14
[T][S]Sparse	+13	+14	+12	+13	+13	+12	+13	+12	+12	+13	+13	+12
step_sgd	+3	+2	+3	+4	+4	+3	+4	+3	+4	+4	+4	+4
step_tween	-0	-1	-0	-0	-1	-1	-0	-1	-1	-0	-1	-0
step_tween_chain	+2	+2	+3	+4	+3	+2	+3	+2	+3	+3	+3	+4
tween	-3	-4	-3	-3	-3	-3	-3	-4	-3	-3	-2	-3
tween_chain	-0	-1	-1	+0	-0	-1	-0	-1	-1	-1	-1	-0

AvailD vs sgd, every mode x dtype (cols 13-24)

AvailD vs sgd, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	-1	+0	-1	-1	-1	-1	-0	-0	-1	-0	-1	-1
Mesh[T]	-4	-3	-3	-4	-3	-4	-3	-4	-3	-4	-4	-4
Mesh[T]Alt	-9	-8	-8	-9	-8	-9	-8	-8	-9	-8	-8	-8
Mesh[T]Chain	-1	-1	-0	-1	-1	-1	-1	-1	-1	-1	-1	-1
Mesh[T][S]	+4	+3	+5	+4	+3	+4	+5	+4	+3	+4	+3	+4
Mesh[T][S][FP]	+3	+3	+5	+4	+3	+4	+5	+4	+3	+5	+3	+4
Mesh[T][S]Sparse	+12	+14	+13	+12	+14	+12	+13	+12	+12	+12	+14	+13
Step[T]Alt	-7	-7	-7	-7	-7	-8	-7	-7	-7	-7	-8	-7
Step[T][S]	-0	+0	+0	-0	+0	+0	+1	-0	+0	-0	-0	+0
Step[T][S][FP]	-1	+0	+1	-0	-0	+0	+1	-0	-1	-0	-1	-0
Step[T][S][HP]	-1	-0	+0	-1	-1	-1	-1	-1	-1	-0	-2	-1
Step[T][S][HP]Async	-0	-0	+1	-1	-1	-0	-0	-0	-1	+0	-0	-0
Step[T][S][L]	+6	+8	+6	+6	+8	+5	+6	+6	+6	+5	+8	+7
Step[T][S][L]Cache	+6	+8	+5	+6	+8	+6	+6	+6	+7	+6	+7	+7
Step[T][S]Sparse	-0	-0	+0	-0	-1	-0	+0	+0	-1	+0	-1	+0
[T]Alt	-9	-8	-8	-8	-8	-8	-8	-8	-8	-8	-8	-8
[T][S]	+3	+3	+5	+4	+3	+4	+5	+4	+3	+4	+2	+4
[T][S][FP]	+3	+3	+5	+3	+3	+4	+5	+4	+3	+4	+3	+4
[T][S][HP]	+4	+3	+5	+4	+3	+4	+5	+4	+3	+4	+3	+4
[T][S][HP]Async	+4	+3	+5	+4	+3	+4	+5	+3	+3	+4	+3	+4
[T][S][L]	+11	+12	+12	+12	+12	+10	+11	+13	+11	+11	+12	+11
[T][S][L]Cache	+13	+14	+13	+13	+15	+12	+13	+13	+13	+12	+15	+13
[T][S]Sparse	+11	+15	+13	+12	+14	+12	+12	+12	+13	+12	+14	+13
step_sgd	+3	+2	+4	+4	+3	+3	+3	+4	+3	+3	+2	+4
step_tween	-1	-0	-1	-1	-1	-1	-0	+0	-1	-0	-2	-1
step_tween_chain	+2	+2	+3	+3	+2	+2	+3	+2	+2	+3	+2	+3
tween	-4	-3	-3	-3	-3	-3	-3	-3	-3	-3	-4	-3
tween_chain	-1	-1	-1	-1	-1	-1	-0	-1	-1	-0	-1	-1

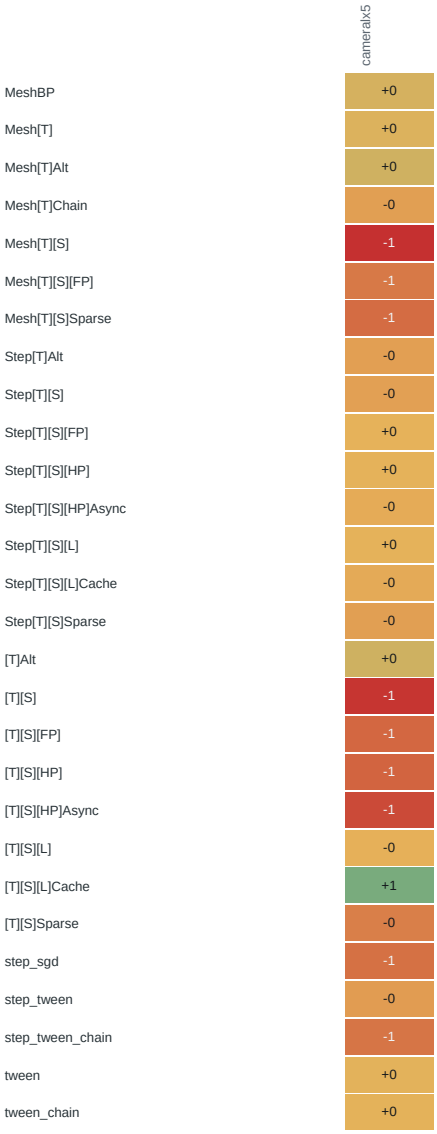
AvailD vs sgd, every mode x dtype (cols 25-34)

AvailD vs sgd, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	-1	-0	-1	-1	-1	-1	-1	-0	-0	-1
Mesh[T]	-4	-3	-3	-3	-4	-3	-3	-3	-4	-3
Mesh[T]Alt	-9	-8	-9	-9	-9	-8	-8	-8	-8	-9
Mesh[T]Chain	-1	-1	-1	-1	-1	-0	-1	-1	-1	-0
Mesh[T][S]	+3	+4	+4	+3	+3	+5	+4	+4	+3	+4
Mesh[T][S][FP]	+3	+4	+4	+4	+3	+5	+5	+4	+3	+5
Mesh[T][S]Sparse	+12	+13	+12	+13	+12	+13	+13	+13	+12	+13
Step[T]Alt	-7	-7	-7	-7	-8	-7	-7	-7	-7	-7
Step[T][S]	-0	-0	+0	+0	-0	+0	+0	-0	-1	-0
Step[T][S][FP]	-1	+1	+0	-1	+0	-0	+0	-0	-1	-0
Step[T][S][HP]	-1	-1	-1	-1	-1	-1	-1	-0	-1	-0
Step[T][S][HP]Async	-0	-0	-0	-0	-0	+0	+0	+0	-1	+0
Step[T][S][L]	+6	+6	+6	+6	+7	+6	+6	+6	+7	+7
Step[T][S][L]Cache	+6	+6	+6	+6	+6	+6	+6	+7	+6	+7
Step[T][S]Sparse	-0	-0	+0	+0	-0	+1	+1	-0	-1	+0
[T]Alt	-9	-8	-9	-8	-9	-8	-8	-9	-9	-8
[T][S]	+3	+3	+5	+3	+3	+5	+5	+4	+3	+4
[T][S][FP]	+4	+4	+4	+4	+4	+5	+5	+4	+3	+4
[T][S][HP]	+4	+4	+5	+3	+3	+4	+5	+4	+3	+4
[T][S][HP]Async	+3	+4	+5	+4	+3	+4	+5	+4	+3	+4
[T][S][L]	+11	+12	+10	+12	+12	+11	+11	+12	+11	+11
[T][S][L]Cache	+13	+13	+13	+13	+13	+13	+13	+13	+13	+13
[T][S]Sparse	+13	+13	+13	+12	+12	+12	+13	+12	+13	+13
step_sgd	+4	+4	+4	+4	+3	+3	+3	+4	+4	+3
step_tween	-1	-0	-0	-1	-1	-1	-0	-0	-1	-0
step_tween_chain	+2	+3	+3	+3	+3	+3	+3	+3	+2	+3
tween	-3	-3	-3	-3	-4	-3	-3	-3	-2	-3
tween_chain	-1	-0	-0	-1	-1	-0	-0	-1	-0	-1

AccD vs sgd, every mode x arch

AccD vs sgd, every mode x arch



Family collapse - Step* vs non-Step

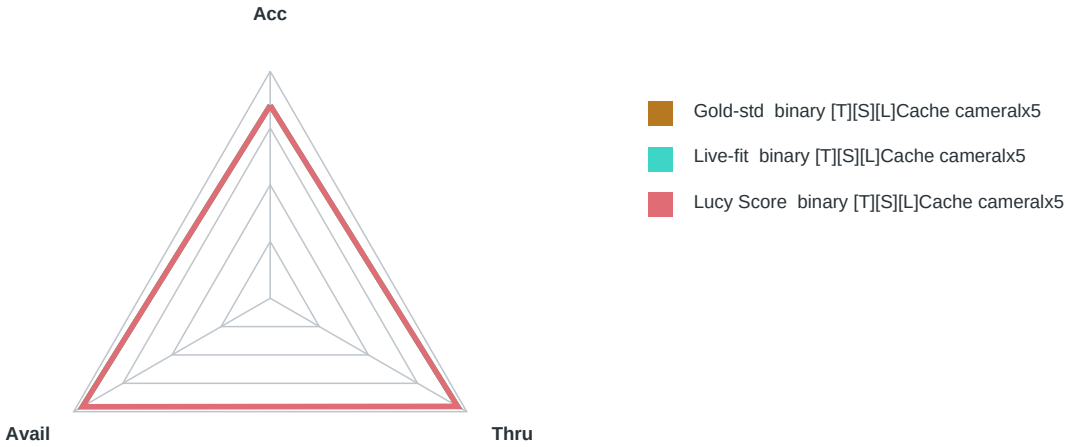
Step* is a 1D pipe (one sample enters layer 0 per tick; output is the sample that entered depth ticks ago). Non-Step of the same family is a full-chain update. AccD is a real scheduler split, not leftover warm-up forwards.

step	plain	n	mean |AccD|
Step[T]Alt	[T]Alt	34	3.57
Step[T][S]	[T][S]	34	2.11
Step[T][S][FP]	[T][S][FP]	34	3.10
Step[T][S][HP]	[T][S][HP]	34	3.17
Step[T][S][HP]Async	[T][S][HP]Async	34	2.65
Step[T][S][L]	[T][S][L]	34	3.37
Step[T][S][L]Cache	[T][S][L]Cache	34	4.37
Step[T][S]Sparse	[T][S]Sparse	34	3.08
step_sgd	sgd	34	1.42
step_tween	tween	34	0.68
step_tween_chain	tween_chain	34	1.56

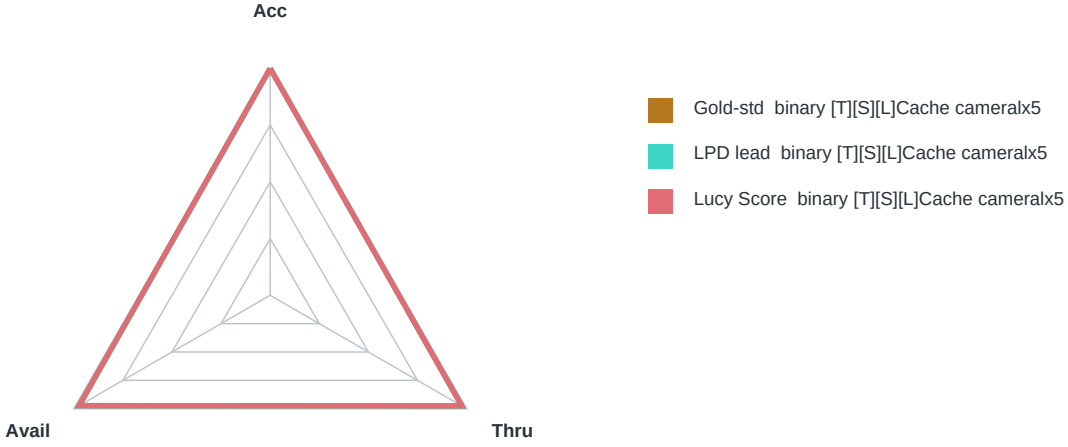
Consciousness - Acc, Throughput, Availability

Synthetic organism / Lucy density: can the net run and train at the same time in a small box. Lucy Score = Throughput x Availability x Acc / 10,000 (hard Acc; SoftAcc is serve-confidence only). SGD that blocks serve dies on Availability. Q = geomean Acc/Thru/Avail vs learner peaks (traps do not set Thru/Avail). LPD = Q x shrink vs Acc-champ RAM; 0 unless Acc keep >=70%. Gold = all 3 pillars >=80% at <=20% Acc-champ RAM. Gold-std = Acc >=80% plus Thru or Avail, then smallest then fastest. Score/MiB is the binary trap.
Acc champ int|none|Step[T][S][HP]|cameralx5|simd Acc 10.8 Thru 217 Avail 23.9% 752.8 KiB (RAM reference)
Lucy Score champ (T x Avail x Acc) binary|none|[T][S][L]Cache|cameralx5|simd Score 28.8 Acc 9.2 Soft 5 11.8 KiB
Live-fit champ (best Q) binary|none|[T][S][L]Cache|cameralx5|simd Acc 9.2 Thru 879 Avail 35.6% 11.8 KiB
Gold-std (2+ pillars, Acc keep >= 80%, then smallest then fastest): binary|none|[T][S][L]Cache|cameralx5|simd mode [T][S][L]Cache Acc 9.2 Thru 879 11.8 KiB
Board fastest float32|none|Mesh[T][S]Sparse|cameralx5|simd Thru 945 (traps may own this) Best availability int|none|[T][S][L]Cache|cameralx5|simd 37.4%
Learner Thru peak 921 learner Avail peak 37.3%

Consciousness radar - Acc / Thru / Avail vs learner peaks



Memory density radar - same pillars x shrink vs Acc champ (traps sit at origin)



Gold - trifecta >=80% at <=20% of Acc-champ RAM

Band	Cell	Acc%	Thru%	Avail%	Q%	RAM%	xSmall	LPD	Acc	Thru	KiB
gold	binary [T][S][L]Cache cameralx5	85	95	96	92	2	32.0	29.39	9.2	879	11.8
gold	ternary [T][S][L]Cache cameralx5	81	98	97	91	3	32.0	29.27	8.7	901	23.5

gold	int2 [T][S][L]Cache cameralx5	82	94	94	90	3	32.0	28.83	8.9	868	23.5
gold	int4 [T][S][L]Cache cameralx5	80	99	97	92	6	16.0	14.69	8.7	911	47.0

Gold-standard train modes - 2+ pillars, Acc keep >= 80%, smallest then fastest

Mode	n	Acc	KiB	Thru	Cell
[T][S][L]Cache	4	9.2	11.8	911	binary [T][S][L]Cache cameralx5 / int4 [T][S][L]Cache cameralx5
Step[T][S][L]	6	9.7	94.1	479	fp8e4m3 Step[T][S][L] cameralx5 / float64 Step[T][S][L] cameralx5
Step[T][S][L]Cache	4	9.4	752.8	479	float64 Step[T][S][L]Cache cameralx5

Near-gold - 2+ pillars, RAM <= 50% of Acc champ

Band	Cell	Acc%	Thru%	Avail%	Q%	RAM%	xSmall	LPD	Acc	Thru	KiB
near	fp8e4m3 Step[T][S][L] cameralx5	85	35	81	62	12	8.0	5.00	9.1	326	94.1
near	float16 Step[T][S][L] cameralx5	81	43	81	65	25	4.0	2.61	8.7	391	188.2

Lucy density (LPD) - Q x shrink vs Acc-champ RAM; 0 if Acc keep < 70%

Band	Cell	Acc%	Thru%	Avail%	Q%	RAM%	xSmall	LPD	Acc	Thru	KiB
gold	binary [T][S][L]Cache cameralx5	85	95	96	92	2	32.0	29.39	9.2	879	11.8
gold	ternary [T][S][L]Cache cameralx5	81	98	97	91	3	32.0	29.27	8.7	901	23.5
gold	int2 [T][S][L]Cache cameralx5	82	94	94	90	3	32.0	28.83	8.9	868	23.5
-	uint2 [T][S][L]Cache cameralx5	73	56	98	74	3	31.9	23.63	7.9	516	23.6
-	int2 MeshBP cameralx5	70	45	56	56	3	32.0	17.93	7.6	412	23.5
gold	int4 [T][S][L]Cache cameralx5	80	99	97	92	6	16.0	14.69	8.7	911	47.0
-	uint3 [T][S][L]Cache cameralx5	77	38	100	66	5	21.3	14.16	8.3	351	35.3
-	int3 [T][S][L]Cache cameralx5	75	36	99	65	5	21.3	13.79	8.1	334	35.3
-	int4 [T][S][L] cameralx5	72	87	91	83	6	16.0	13.26	7.8	805	47.0
-	int3 [T][S][L] cameralx5	71	33	95	61	5	21.3	12.96	7.6	307	35.3
-	nf4 [T][S][L]Cache cameralx5	79	44	97	70	6	16.0	11.17	8.5	408	47.0
-	uint5 [T][S][L]Cache cameralx5	72	32	99	61	8	12.8	7.79	7.8	291	58.9
-	int5 [T][S][L]Cache cameralx5	72	30	100	60	8	12.8	7.68	7.8	278	58.8
-	int8 [T][S][L]Cache cameralx5	77	100	97	91	12	8.0	7.27	8.4	921	94.1
-	uint8 [T][S][L]Cache cameralx5	76	90	99	88	13	8.0	7.00	8.2	826	94.1
-	int6 [T][S][L]Cache cameralx5	71	28	100	58	9	10.7	6.19	7.7	254	70.6
-	uint8 Mesh[T][S][FP] cameralx5	71	51	71	64	13	8.0	5.09	7.6	473	94.1
-	fp8e5m2 Step[T][S][L] cameralx5	73	42	81	63	12	8.0	5.03	7.9	386	94.1
near	fp8e4m3 Step[T][S][L] cameralx5	85	35	81	62	12	8.0	5.00	9.1	326	94.1
-	fp8e5m2 Step[T][S][L]Cache cameralx5	71	40	80	61	12	8.0	4.89	7.7	372	94.1

Consciousness rank - Q = geomean Acc/Thru/Avail keep

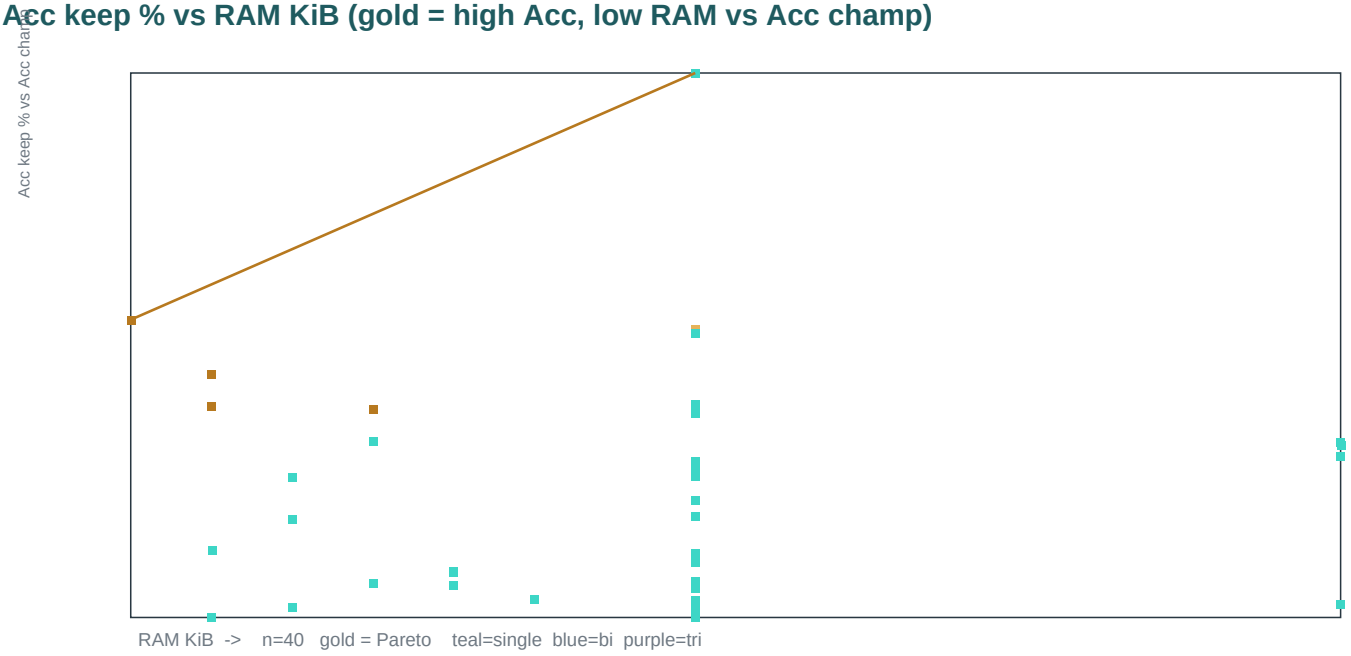
Band	Cell	Acc%	Thru%	Avail%	Q%	LPD	Thru	Avail
gold	binary [T][S][L]Cache cameralx5	85	95	96	92	29.39	879	35.6
gold	int4 [T][S][L]Cache cameralx5	80	99	97	92	14.69	911	36.3
gold	ternary [T][S][L]Cache cameralx5	81	98	97	91	29.27	901	36.2
-	int8 [T][S][L]Cache cameralx5	77	100	97	91	7.27	921	36.2
gold	int2 [T][S][L]Cache cameralx5	82	94	94	90	28.83	868	35.1
-	uint8 [T][S][L]Cache cameralx5	76	90	99	88	7.00	826	36.7
-	int4 [T][S][L] cameralx5	72	87	91	83	13.26	805	33.8
acc	float32 Step[T][S][L]Cache cameralx5	87	70	80	79	1.57	643	29.8
-	uint16 [T][S][L]Cache cameralx5	79	59	98	77	3.08	543	36.6
-	int16 [T][S][L]Cache cameralx5	78	57	100	76	3.05	524	37.2

Trap - tiny RAM, Acc keep < 70% (Score/MiB and SoftAcc Score lie here)

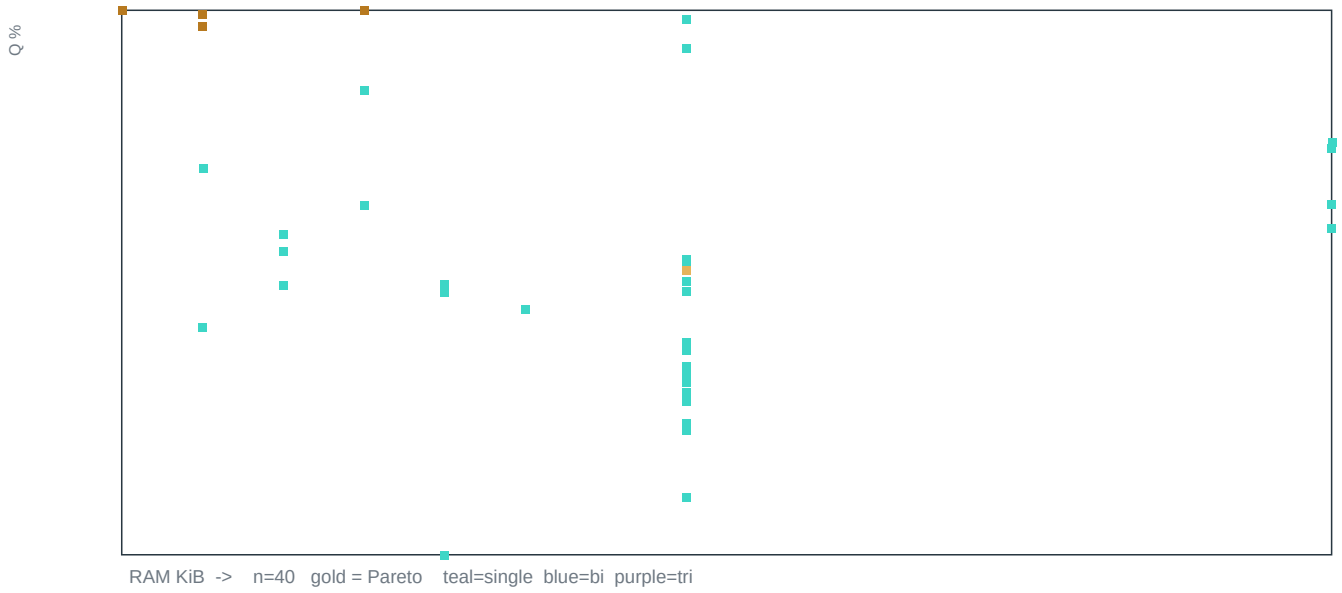
Band	Cell	Acc%	Thru%	Avail%	Q%	RAM%	xSmall	LPD	Acc	Thru	KiB

Band	Cell	Acc%	Thru%	Avail%	Q%	RAM%	xSmall	LPD	Acc	Thru	KiB
trap	binary sgd cameralx5	58	50	58	55	2	32.0	0.00	6.3	459	11.8
trap	binary step_sgd cameralx5	60	56	64	60	2	32.0	0.00	6.5	513	11.8
trap	binary tween cameralx5	21	36	48	33	2	32.0	0.00	2.3	332	11.8
trap	binary tween_chain cameralx5	31	46	56	43	2	32.0	0.00	3.3	422	11.8
trap	binary step_tween cameralx5	15	41	54	32	2	32.0	0.00	1.7	381	11.8
trap	binary step_tween_chain cameralx5	43	52	63	52	2	32.0	0.00	4.7	481	11.8
trap	binary MeshBP cameralx5	63	43	55	53	2	32.0	0.00	6.8	397	11.8
trap	binary Mesh[T] cameralx5	20	34	48	32	2	32.0	0.00	2.1	315	11.8
trap	binary Mesh[T]Chain cameralx5	29	43	56	41	2	32.0	0.00	3.1	394	11.8
trap	binary [T][S] cameralx5	51	54	66	57	2	32.0	0.00	5.5	499	11.8

Acc keep % vs RAM KiB (gold = high Acc, low RAM vs Acc champ)

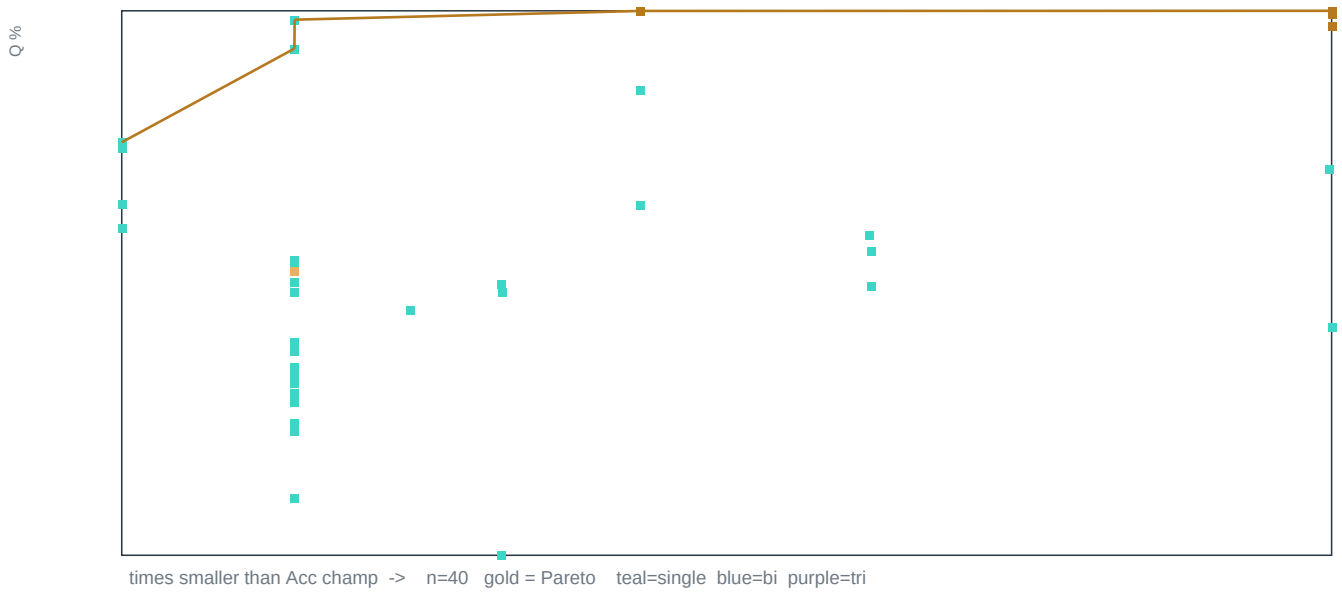


Q% vs RAM KiB (gold = high consciousness, low RAM)

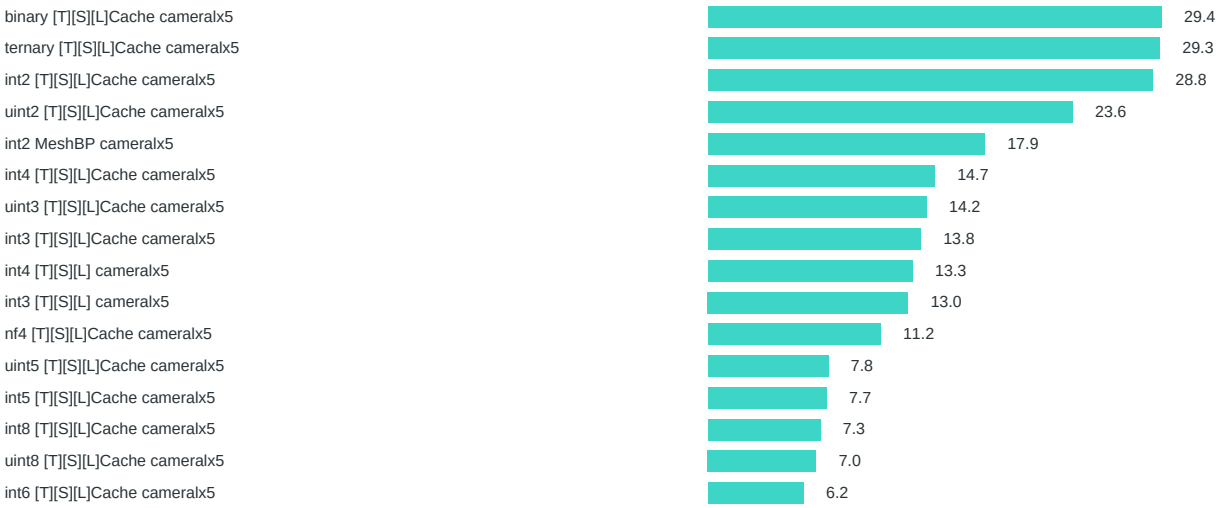


Q% vs shrink vs Acc champ (gold = upper right)

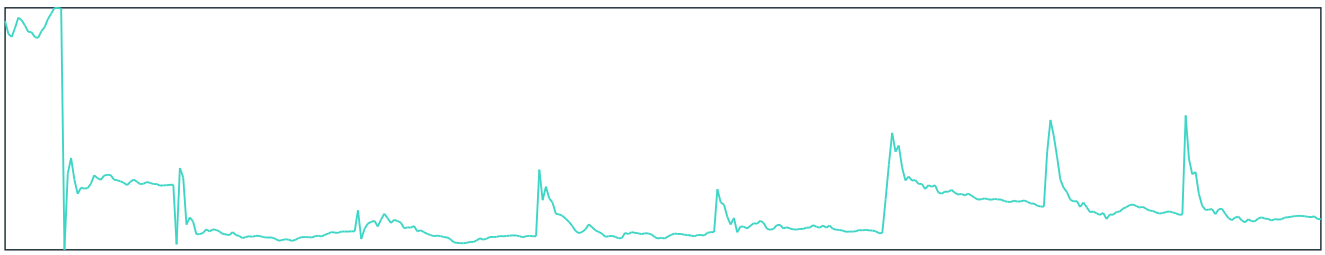
Q% vs shrink vs Acc champ (gold = upper right)



Top Lucy density (LPD)



Live pulse (Score)



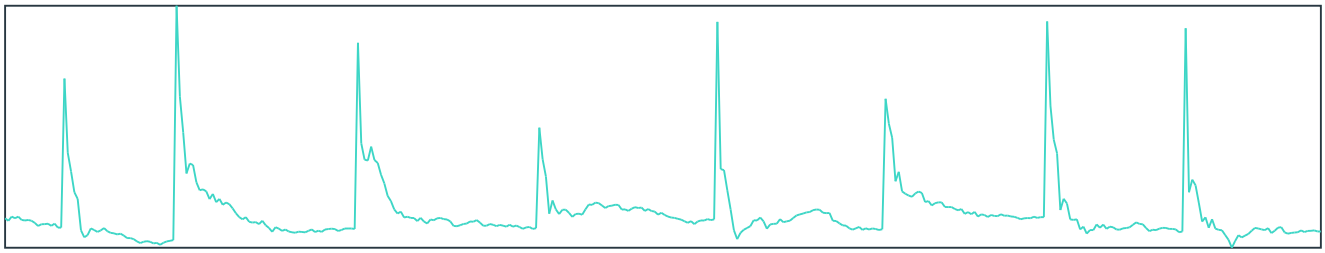
n=400 min=1.16 max=5.15

Live pulse (SoftAcc)



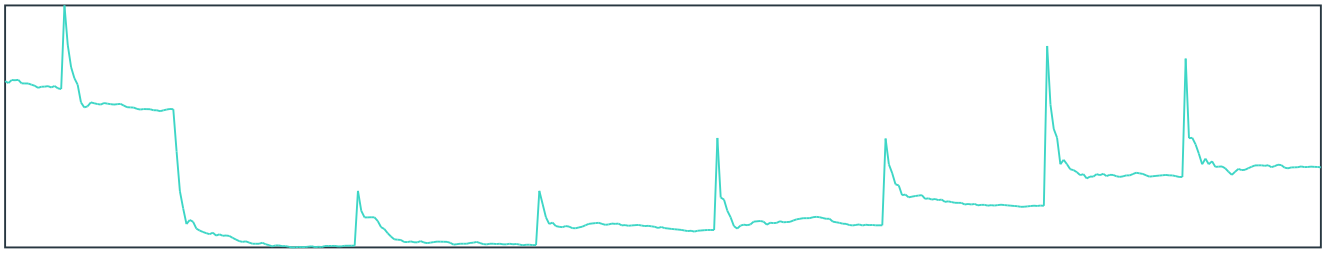
n=400 min=1.54 max=2.41

Live pulse (Availability)



n=400 min=23.86 max=31.42

Live pulse (Throughput)



n=400 min=125.77 max=271.82

Queue by train mode (this epoch)

Mode	Done	Run	Left	Total
sgd	34	0	0	34
step_sgd	34	0	0	34
tween	34	0	0	34
tween_chain	34	0	0	34
step_tween	34	0	0	34
step_tween_chain	34	0	0	34
MeshBP	34	0	0	34
Mesh[T]	34	0	0	34
Mesh[T]Chain	34	0	0	34
[T][S]	34	0	0	34
Step[T][S]	34	0	0	34
[T]Alt	34	0	0	34
Step[T]Alt	34	0	0	34
[T][S][HP]	34	0	0	34
[T][S][L]	34	0	0	34
[T][S][FP]	34	0	0	34
[T][S][L]Cache	34	0	0	34
[T][S][HP]Async	34	0	0	34
[T][S]Sparse	34	0	0	34
Mesh[T][S]	34	0	0	34
Mesh[T]Alt	34	0	0	34
Mesh[T][S][FP]	34	0	0	34
Mesh[T][S]Sparse	34	0	0	34
Step[T][S][HP]	34	0	0	34
Step[T][S][L]	34	0	0	34
Step[T][S][FP]	34	0	0	34
Step[T][S][L]Cache	34	0	0	34
Step[T][S][HP]Async	34	0	0	34

Step[T][S]Sparse	34	0	0	34