tide GPT-char

Lucy Score = Throughput x Availability x Acc / 10,000. LPD condenses live-fit vs Acc-champ RAM.
[T]=Tween [S]=Split [FP]=FastProxy [L]=Linear [HP]=HeadProxy
done - epoch 1 - lr 20 - 2026-08-21 09:03:13 - 0.0.0.0:8155
This epoch 986 / 986 cells. Recorded 986 results. Learning rate 20.
Score 0 usually means the cell finished before a Lucy pulse (Acc never sampled). Score is live-fit: Throughput x Availability x Acc.
SGD that blocks serve dies on Availability. SoftAcc is serve-confidence only.
live_gpt v1.0.0 - cameralx5 - tinyshakespeare - 4096 windows - seq 32 - causal MHA - A->B->A2 - SIMD

Lucy champions (this tide)

Axis	Cell	Score	Soft	Acc	Thru	Avail
hard acc	int64|none|Mesh[T]Chain|cameralx5|simd	3.42	6.1	6.1	233.3	24.0
throughput	float32|none|[T][S][L]|cameralx5|simd	9.03	0.0	2.7	917.4	36.2
availability	fp6|none|[T][S][L]Cache|cameralx5|simd	7.19	4.6	7.9	245.3	37.3
lucy score	int4|none|[T][S][L]Cache|cameralx5|simd	28.79	4.8	9.4	858.2	35.8
mobile score (trap)	binary|none|Mesh[T][S]Sparse|cameralx5|simd	19.79	4.1	6.5	857.4	35.5
acc/sec	int4|none|[T][S][L]Cache|cameralx5|simd	28.79	4.8	9.4	858.2	35.8

Lucy axis champions (this tide)

Axis	Mode	DType	Arch	Value
hard_acc	Step[T][S][L]	int64	cameralx5	10.60
throughput	[T][S][L]	float32	cameralx5	917.38
availability	[T][S][L]Cache	fp6	cameralx5	37.28
score	[T][S][L]Cache	int4	cameralx5	28.79
soft_acc	Mesh[T]Chain	int64	cameralx5	6.12
acc_thru	[T][S][L]Cache	int4	cameralx5	80.41
realtime	[T][S][L]	float32	cameralx5	331.72
adapt	Mesh[T]Alt	fp8e4m3	cameralx5	6.23
keep_learn	Mesh[T][S]Sparse	int4	cameralx5	10.44
acc_per_sec	[T][S][L]Cache	int4	cameralx5	1.27
consistency	Mesh[T]Chain	int64	cameralx5	10.00
stability	sgd	fp4	cameralx5	100.00
mobile_score	Mesh[T][S]Sparse	binary	cameralx5	1722.67
lpd	[T][S][L]Cache	int2	cameralx5	29.26
mspeed	[T][S][L]Cache	int8	cameralx5	1.00
mavail	[T][S][L]Cache	fp6	cameralx5	1.00
mix	[T][S][L]Cache	int4	cameralx5	0.95
gold_std	[T][S][L]Cache	int2	cameralx5	23.52

Best settings per train mode

Mode	DType	Format	Score	Soft	Acc	Avail	n
[T][S][L]Cache	int4	none	28.8	4.8	9.4	35.8	34
Mesh[T][S]Sparse	int2	none	20.5	4.4	7.1	34.9	34
[T][S][L]	int4	none	19.7	4.6	7.5	34.0	34
[T][S]Sparse	int2	none	19.5	4.5	6.6	35.1	34
Step[T][S][L]Cache	float32	none	17.5	1.6	9.3	29.6	34
Step[T][S][L]	float32	none	16.2	1.6	8.2	30.1	34
[T][S]	int8	none	10.0	4.5	7.2	26.4	34
step_sgd	int8	none	9.8	4.4	6.7	26.2	34
Mesh[T][S]	int8	none	9.7	4.6	7.2	26.1	34
Step[T][S][FP]	float32	none	9.2	1.6	9.3	22.9	34
Step[T][S][HP]	float32	none	9.0	1.6	9.3	22.7	34

step_tween	float32	none	8.7	1.6	8.5	23.2	34
Step[T][S]Sparse	float32	none	8.7	1.6	8.8	22.8	34
Step[T][S][HP]Async	float32	none	8.7	1.6	8.6	23.0	34
[T][S][HP]Async	uint8	none	8.5	4.1	6.8	26.7	34
Step[T][S]	float32	none	8.3	1.6	8.4	23.0	34
Mesh[T][S][FP]	int2	none	8.0	4.4	6.9	24.5	34
[T][S][FP]	int2	none	8.0	4.5	7.3	24.1	34
tween	float32	none	7.6	1.6	9.4	20.6	34
sgd	float32	none	7.4	5.5	5.4	23.9	34
step_tween_chain	int2	none	7.3	4.3	7.2	23.1	34
Mesh[T]	float32	none	7.2	1.6	9.9	20.1	34
tween_chain	uint8	none	6.9	4.4	7.0	24.0	34
MeshBP	int8	none	6.7	4.2	7.0	22.7	34
Mesh[T]Chain	int8	none	6.6	4.5	6.7	23.0	34
[T][S][HP]	int8	none	5.1	1.7	3.9	26.1	34
Step[T]Alt	float32	none	3.9	1.6	8.6	16.5	34
[T]Alt	float32	none	2.8	0.0	2.7	23.0	34
Mesh[T]Alt	float32	none	2.7	0.0	2.6	22.9	34

Best dtype per mode

Mode	Winner dtype	Score	Soft	Acc
[T][S][L]Cache	int4	28.8	4.8	9.4
Mesh[T][S]Sparse	int2	20.5	4.4	7.1
[T][S][L]	int4	19.7	4.6	7.5
[T][S]Sparse	int2	19.5	4.5	6.6
Step[T][S][L]Cache	float32	17.5	1.6	9.3
Step[T][S][L]	float32	16.2	1.6	8.2
[T][S]	int8	10.0	4.5	7.2
step_sgd	int8	9.8	4.4	6.7
Mesh[T][S]	int8	9.7	4.6	7.2
Step[T][S][FP]	float32	9.2	1.6	9.3
Step[T][S][HP]	float32	9.0	1.6	9.3
step_tween	float32	8.7	1.6	8.5
Step[T][S]Sparse	float32	8.7	1.6	8.8
Step[T][S][HP]Async	float32	8.7	1.6	8.6
[T][S][HP]Async	uint8	8.5	4.1	6.8
Step[T][S]	float32	8.3	1.6	8.4
Mesh[T][S][FP]	int2	8.0	4.4	6.9
[T][S][FP]	int2	8.0	4.5	7.3
tween	float32	7.6	1.6	9.4
sgd	float32	7.4	5.5	5.4
step_tween_chain	int2	7.3	4.3	7.2
Mesh[T]	float32	7.2	1.6	9.9
tween_chain	uint8	6.9	4.4	7.0
MeshBP	int8	6.7	4.2	7.0
Mesh[T]Chain	int8	6.6	4.5	6.7
[T][S][HP]	int8	5.1	1.7	3.9
Step[T]Alt	float32	3.9	1.6	8.6
[T]Alt	float32	2.8	0.0	2.7
Mesh[T]Alt	float32	2.7	0.0	2.6

Best mode per dtype

DType	Winner mode	Score	Soft	Acc
int4	[T][S][L]Cache	28.8	4.8	9.4
int2	[T][S][L]Cache	26.0	4.4	8.8
int8	[T][S][L]Cache	25.2	4.5	8.2
uint8	[T][S][L]Cache	25.2	4.6	8.8
ternary	Mesh[T][S]Sparse	19.9	4.2	6.6
binary	Mesh[T][S]Sparse	19.8	4.1	6.5
float32	Step[T][S][L]Cache	17.5	1.6	9.3
uint32	[T][S][L]Cache	17.3	4.7	8.9
uint16	[T][S][L]Cache	16.5	4.8	8.5
uint4	[T][S][L]Cache	16.5	4.7	8.5
uint64	[T][S][L]Cache	14.8	4.4	7.6
uint	[T][S][L]Cache	14.6	4.7	8.6
int32	[T][S][L]Cache	13.9	4.7	8.2
int16	[T][S][L]Cache	13.5	4.5	7.9
uintptr	[T][S][L]Cache	13.5	4.6	7.9
float64	Step[T][S][L]Cache	13.0	1.6	8.5
bfloat16	Step[T][S][L]Cache	12.2	1.6	8.2
float16	Step[T][S][L]	12.0	1.6	9.7
uint2	Mesh[T][S]Sparse	11.8	3.9	6.4
nf4	[T][S][L]Cache	11.3	4.6	8.1
uint3	[T][S][L]Cache	10.7	4.5	8.6
int64	Step[T][S][L]	10.6	1.7	10.6
int3	[T][S][L]Cache	10.0	4.4	8.4
fp8e5m2	Step[T][S][L]	9.9	1.6	9.1
int	Step[T][S][L]Cache	9.6	1.6	10.0
fp8e4m3	Step[T][S][L]	8.9	1.6	8.9
complex128	Step[T][S][L]Cache	8.3	1.6	8.6
complex64	Step[T][S][L]Cache	8.1	1.6	8.6
uint5	[T][S][L]Cache	8.0	4.6	7.8
uint6	[T][S][L]Cache	7.8	4.5	8.1
int5	[T][S][L]Cache	7.7	4.5	8.0
int6	[T][S][L]Cache	7.5	4.6	8.3
fp6	[T][S][L]Cache	7.2	4.6	7.9
fp4	[T][S][L]Cache	6.3	1.5	2.5

Leaderboard (Lucy Score)

#	Cell	Score	Soft	Acc	Thru	Avail
1	int4|none|[T][S][L]Cache|cameralx5|simd	28.8	4.8	9.4	858.2	35.8
2	int2|none|[T][S][L]Cache|cameralx5|simd	26.0	4.4	8.8	840.2	35.1
3	int8|none|[T][S][L]Cache|cameralx5|simd	25.2	4.5	8.2	859.4	35.8
4	uint8|none|[T][S][L]Cache|cameralx5|simd	25.2	4.6	8.8	785.4	36.4
5	int2|none|Mesh[T][S]Sparse|cameralx5|simd	20.5	4.4	7.1	831.3	34.9
6	ternary|none|Mesh[T][S]Sparse|cameralx5|simd	19.9	4.2	6.6	853.6	35.3
7	binary|none|Mesh[T][S]Sparse|cameralx5|simd	19.8	4.1	6.5	857.4	35.5
8	int4|none|[T][S][L]|cameralx5|simd	19.7	4.6	7.5	775.3	34.0
9	int8|none|[T][S][L]|cameralx5|simd	19.7	4.6	7.5	779.4	33.7
10	int2|none|[T][S]Sparse|cameralx5|simd	19.5	4.5	6.6	839.8	35.1
11	ternary|none|[T][S]Sparse|cameralx5|simd	18.5	4.2	6.4	823.6	35.1
12	int8|none|[T][S]Sparse|cameralx5|simd	17.8	3.9	5.9	857.3	35.4
13	float32|none|Step[T][S][L]Cache|cameralx5|simd	17.5	1.6	9.3	634.0	29.6
14	int2|none|[T][S][L]|cameralx5|simd	17.5	4.3	7.1	742.0	33.0

15	uint32|none|[T][S][L]Cache|cameralx5|simd	17.3	4.7	8.9	528.4	36.8
16	uint8|none|Mesh[T][S]Sparse|cameralx5|simd	17.0	3.9	5.8	802.3	36.6
17	int4|none|Mesh[T][S]Sparse|cameralx5|simd	16.9	4.0	5.5	857.1	35.6
18	uint8|none|[T][S][L]|cameralx5|simd	16.5	4.6	7.0	691.4	34.1
19	uint16|none|[T][S][L]Cache|cameralx5|simd	16.5	4.8	8.5	530.0	36.8
20	uint4|none|[T][S][L]Cache|cameralx5|simd	16.5	4.7	8.5	527.2	36.8

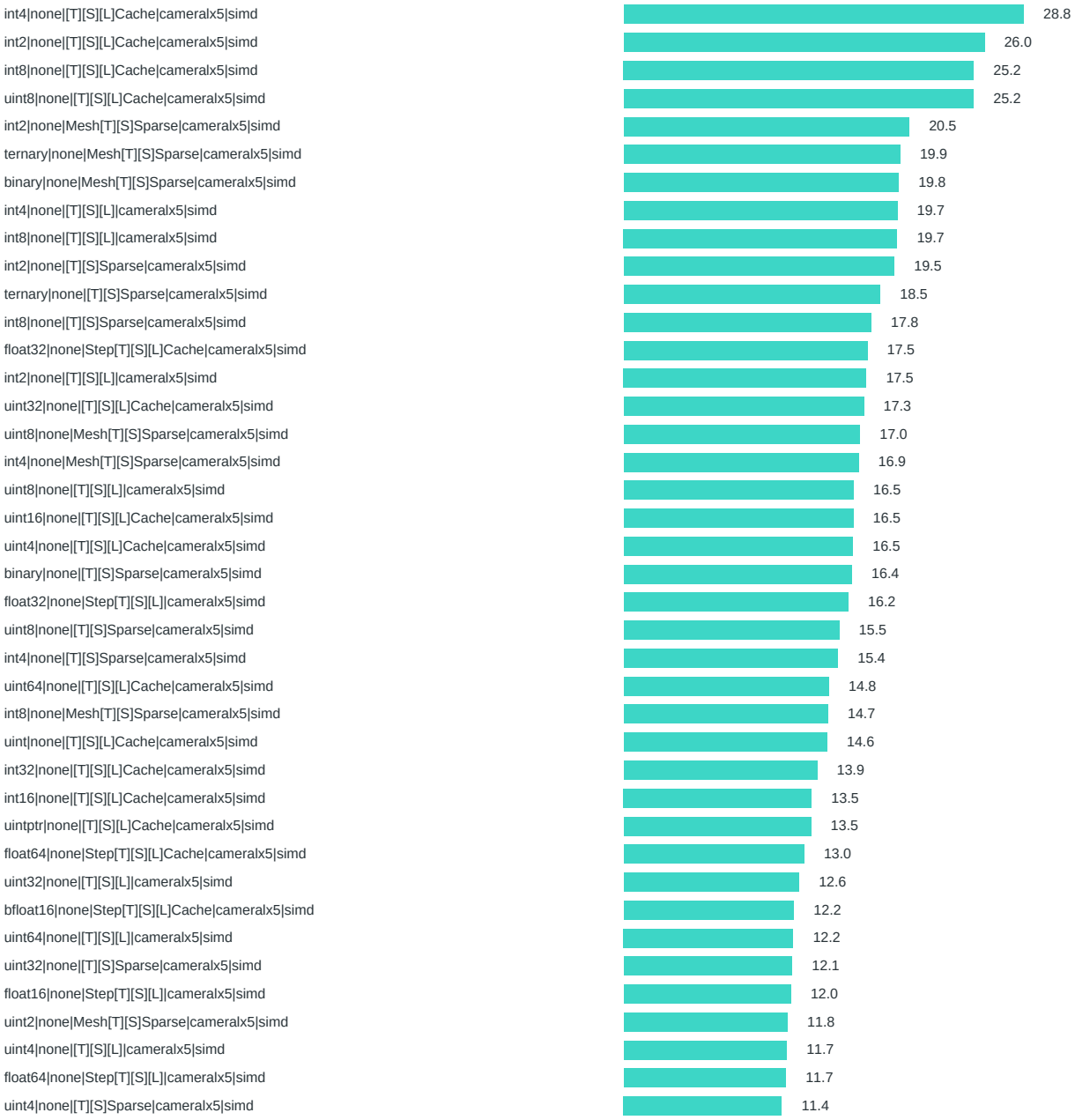
Leaderboard (SoftAcc)

#	Cell	Score	Soft	Acc	Thru	Avail
1	int4|none|[T][S][L]Cache|cameralx5|simd	28.8	4.8	9.4	858.2	35.8
2	uint16|none|[T][S][L]Cache|cameralx5|simd	16.5	4.8	8.5	530.0	36.8
3	uint4|none|[T][S][L]Cache|cameralx5|simd	16.5	4.7	8.5	527.2	36.8
4	int32|none|[T][S][L]Cache|cameralx5|simd	13.9	4.7	8.2	462.6	36.8
5	uint|none|[T][S][L]Cache|cameralx5|simd	14.6	4.7	8.6	459.1	36.9
6	uint32|none|[T][S][L]Cache|cameralx5|simd	17.3	4.7	8.9	528.4	36.8
7	uint8|none|[T][S][L]|cameralx5|simd	16.5	4.6	7.0	691.4	34.1
8	int4|none|[T][S][L]|cameralx5|simd	19.7	4.6	7.5	775.3	34.0
9	int8|none|[T][S][L]|cameralx5|simd	19.7	4.6	7.5	779.4	33.7
10	uintptr|none|[T][S][L]Cache|cameralx5|simd	13.5	4.6	7.9	461.8	37.0
11	uint8|none|[T][S][L]Cache|cameralx5|simd	25.2	4.6	8.8	785.4	36.4
12	int16|none|[T][S][L]Cache|cameralx5|simd	13.5	4.5	7.9	468.7	36.5
13	int8|none|[T][S][L]Cache|cameralx5|simd	25.2	4.5	8.2	859.4	35.8
14	uint32|none|[T][S][L]|cameralx5|simd	12.6	4.5	7.0	499.2	35.8
15	int2|none|[T][S]Sparse|cameralx5|simd	19.5	4.5	6.6	839.8	35.1
16	int2|none|Mesh[T][S]Sparse|cameralx5|simd	20.5	4.4	7.1	831.3	34.9
17	int2|none|[T][S][L]Cache|cameralx5|simd	26.0	4.4	8.8	840.2	35.1
18	uint64|none|[T][S][L]Cache|cameralx5|simd	14.8	4.4	7.6	528.8	36.7
19	uint64|none|[T][S][L]|cameralx5|simd	12.2	4.3	6.7	506.5	35.8
20	int2|none|[T][S][L]|cameralx5|simd	17.5	4.3	7.1	742.0	33.0

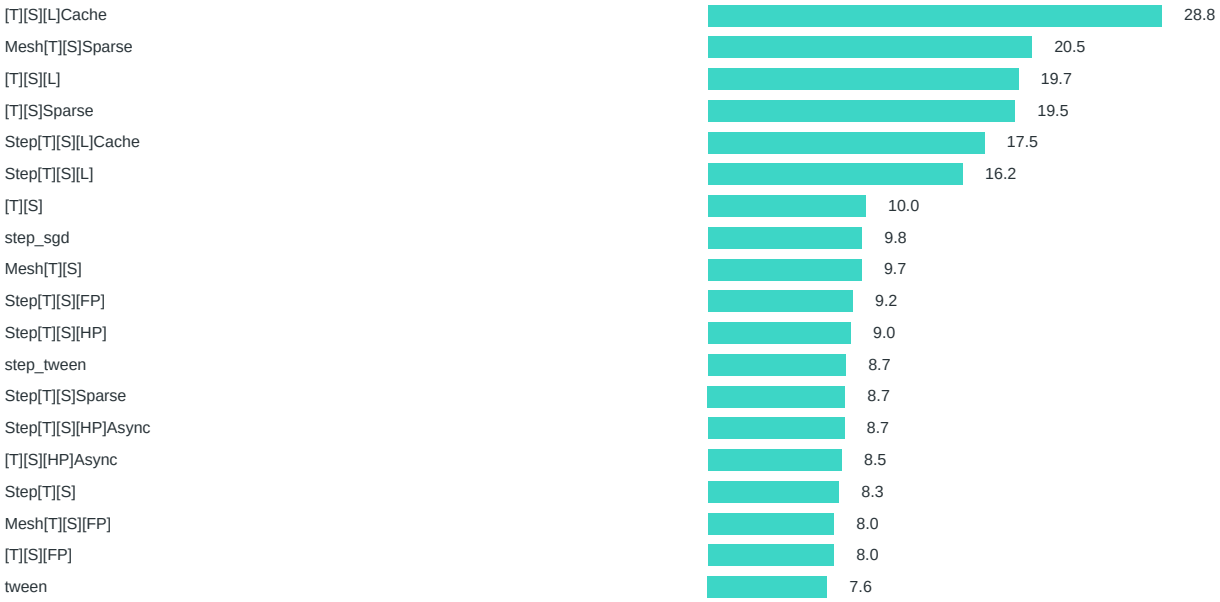
Leaderboard (hard Acc)

#	Cell	Score	Soft	Acc	Thru	Avail
1	float16|none|Step[T][S][L]|cameralx5|simd	12.0	1.6	9.7	401.5	30.8
2	int4|none|[T][S][L]Cache|cameralx5|simd	28.8	4.8	9.4	858.2	35.8
3	float32|none|Step[T][S][L]Cache|cameralx5|simd	17.5	1.6	9.3	634.0	29.6
4	uint32|none|[T][S][L]Cache|cameralx5|simd	17.3	4.7	8.9	528.4	36.8
5	int2|none|[T][S][L]Cache|cameralx5|simd	26.0	4.4	8.8	840.2	35.1
6	uint8|none|[T][S][L]Cache|cameralx5|simd	25.2	4.6	8.8	785.4	36.4
7	uint|none|[T][S][L]Cache|cameralx5|simd	14.6	4.7	8.6	459.1	36.9
8	float64|none|Step[T][S][L]Cache|cameralx5|simd	13.0	1.6	8.5	494.5	30.8
9	uint4|none|[T][S][L]Cache|cameralx5|simd	16.5	4.7	8.5	527.2	36.8
10	uint16|none|[T][S][L]Cache|cameralx5|simd	16.5	4.8	8.5	530.0	36.8
11	bfloat16|none|Step[T][S][L]Cache|cameralx5|simd	12.2	1.6	8.2	492.0	30.2
12	float32|none|Step[T][S][L]|cameralx5|simd	16.2	1.6	8.2	652.2	30.1
13	int8|none|[T][S][L]Cache|cameralx5|simd	25.2	4.5	8.2	859.4	35.8
14	int32|none|[T][S][L]Cache|cameralx5|simd	13.9	4.7	8.2	462.6	36.8
15	float64|none|Step[T][S][L]|cameralx5|simd	11.7	1.6	8.1	475.9	30.3
16	int16|none|[T][S][L]Cache|cameralx5|simd	13.5	4.5	7.9	468.7	36.5
17	uintptr|none|[T][S][L]Cache|cameralx5|simd	13.5	4.6	7.9	461.8	37.0
18	uint64|none|[T][S][L]Cache|cameralx5|simd	14.8	4.4	7.6	528.8	36.7
19	int8|none|[T][S][L]|cameralx5|simd	19.7	4.6	7.5	779.4	33.7
20	int4|none|[T][S][L]|cameralx5|simd	19.7	4.6	7.5	775.3	34.0

Top scores



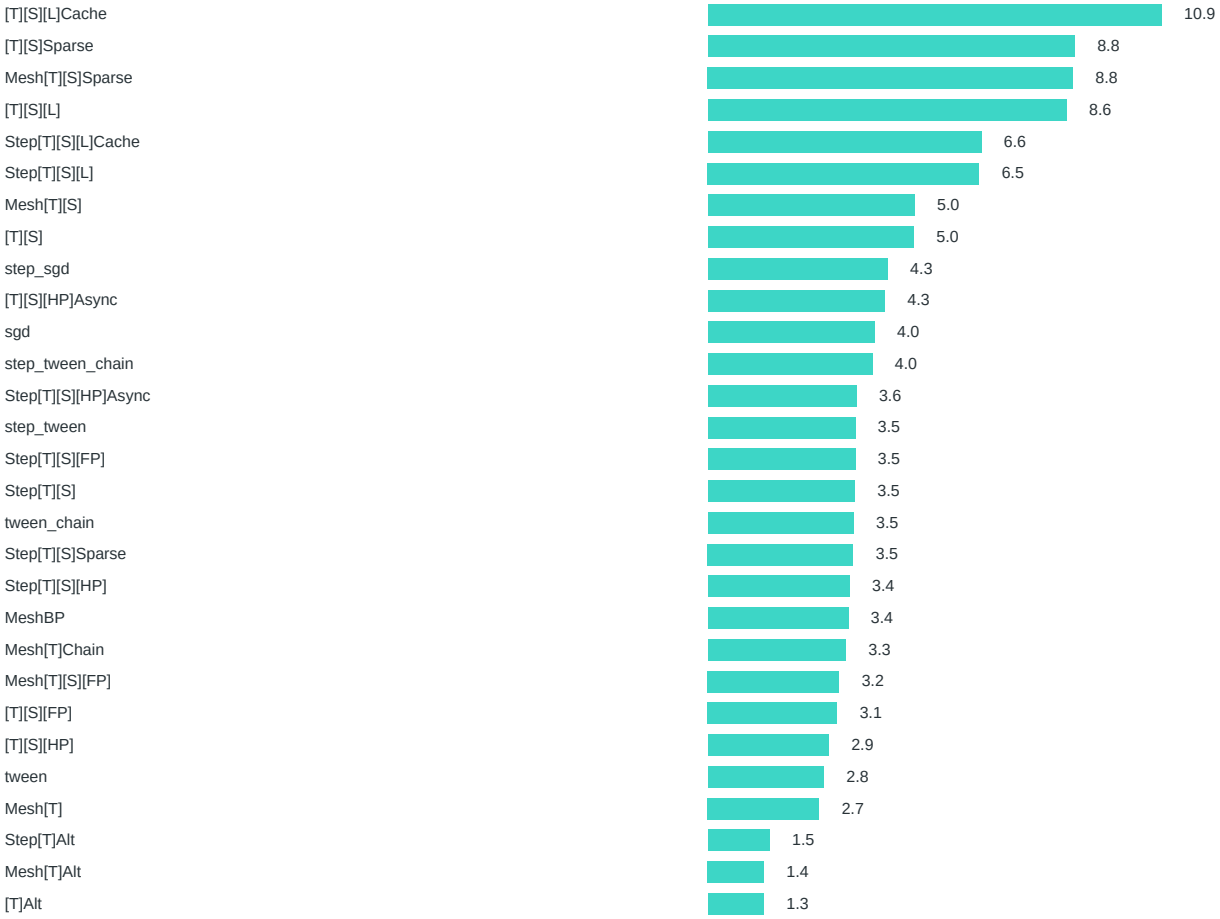
Best settings per mode



Best settings per mode



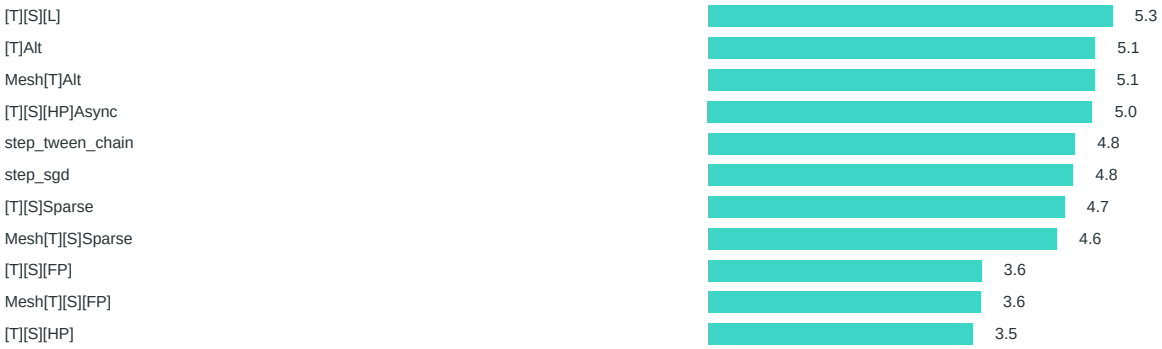
Mean Score by train mode



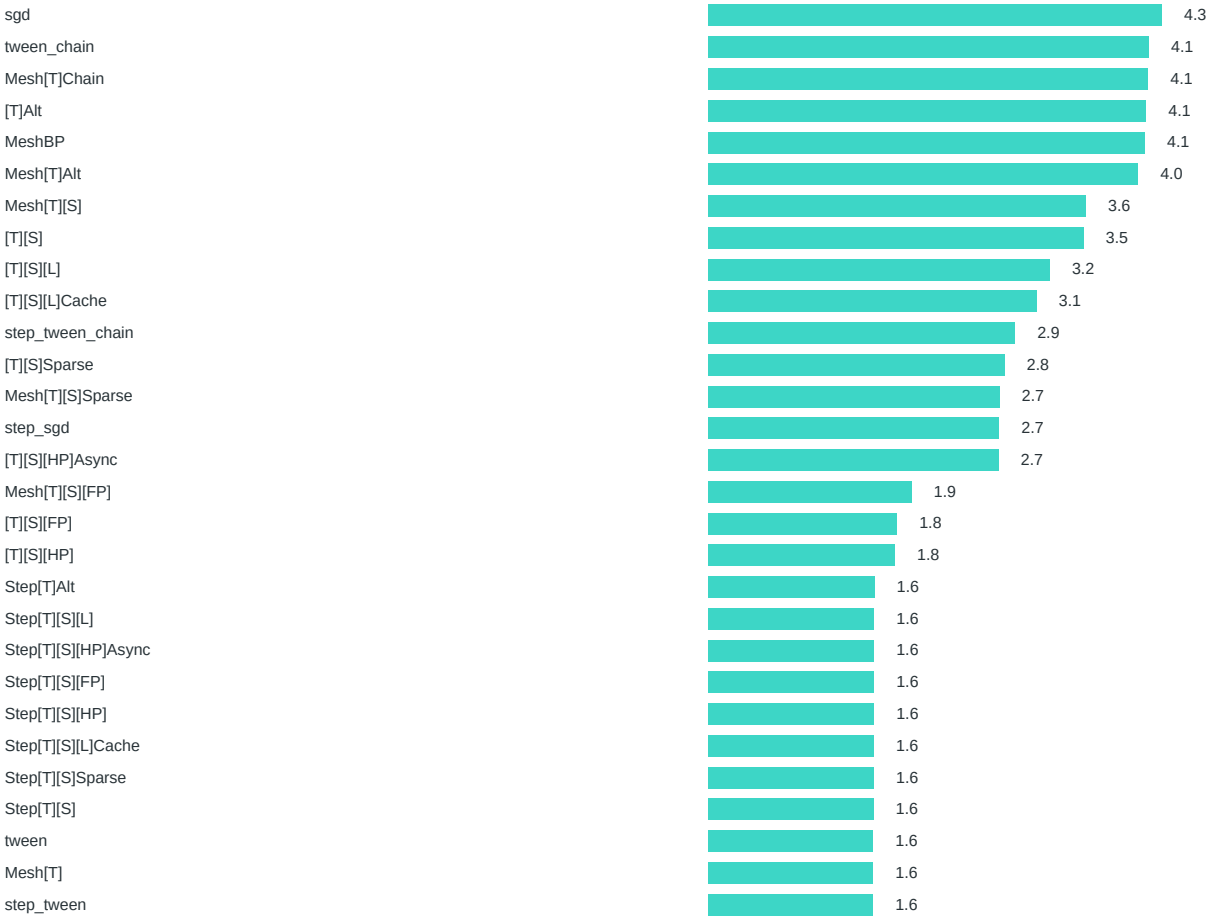
Mean hard Acc by train mode



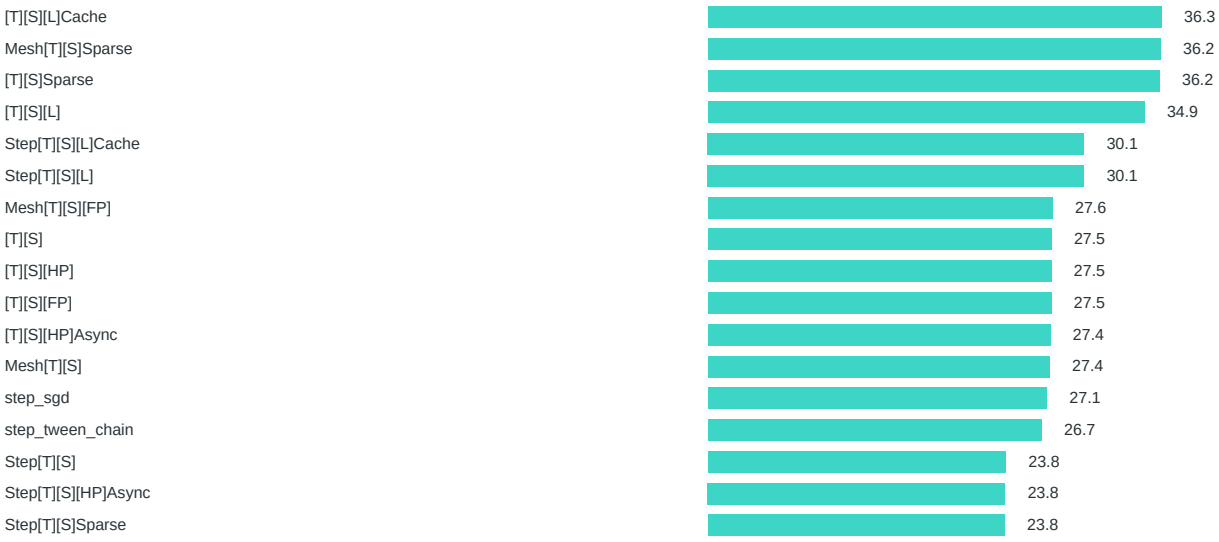
Mean hard Acc by train mode



Mean SoftAcc by train mode



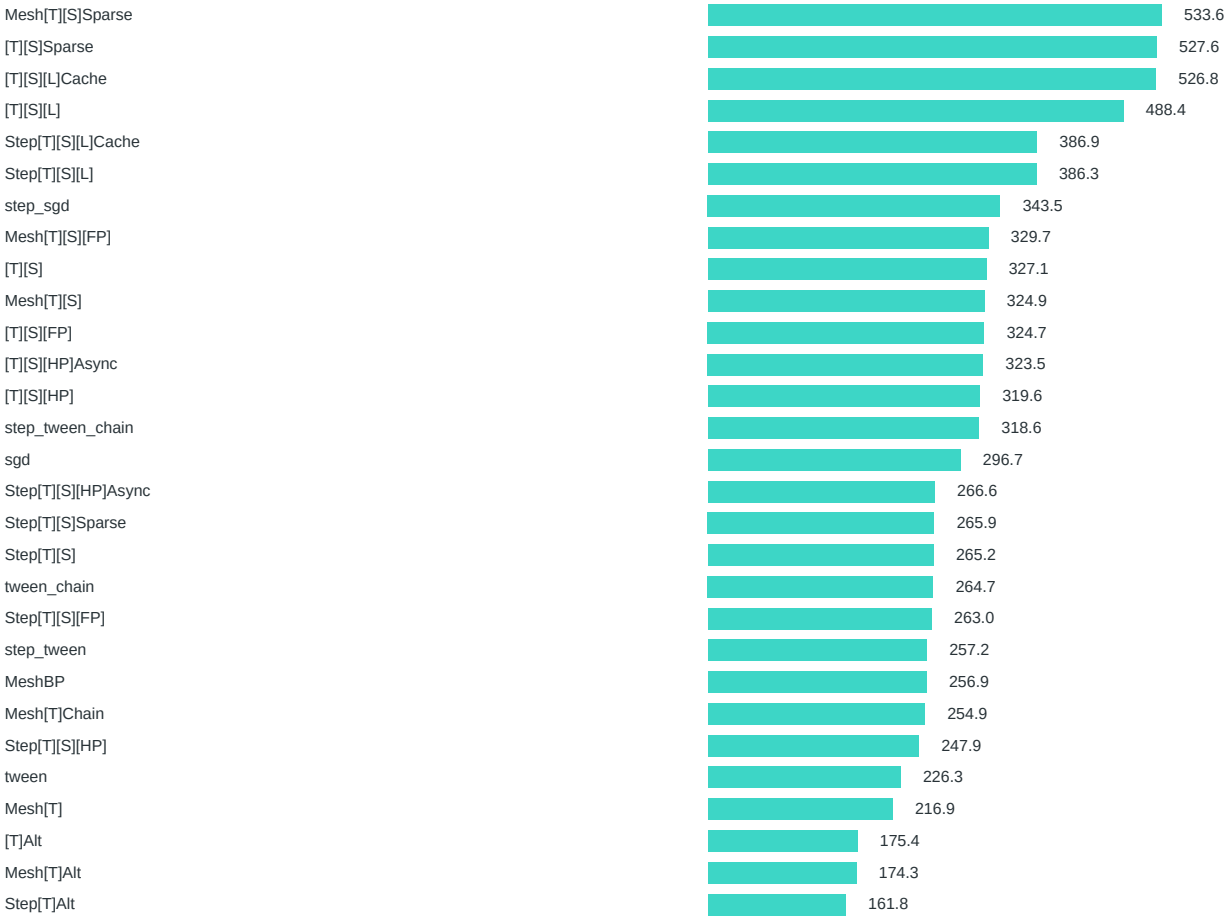
Mean Availability by train mode



Mean Availability by train mode



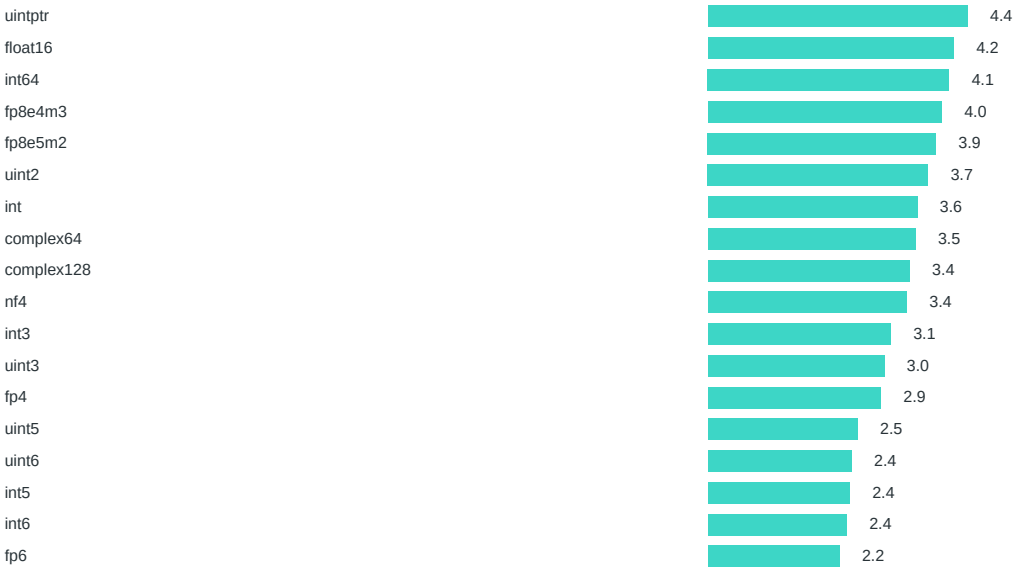
Mean Throughput by train mode



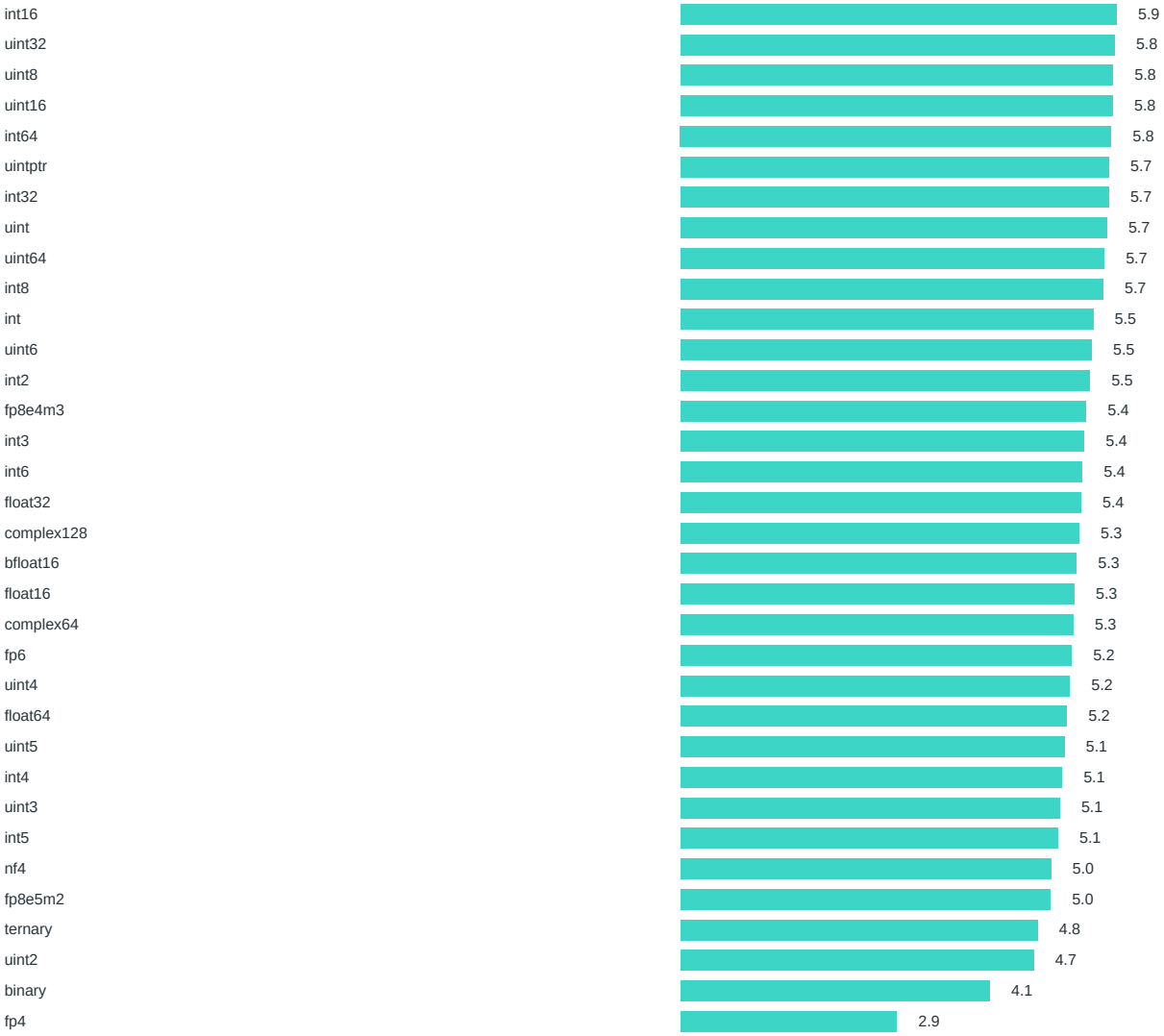
Mean Score by dtype



Mean Score by dtype



Mean hard Acc by dtype



Mean Score by arch



Honesty - mean Score, every mode x dtype (cols 1-12)

Honesty - mean Score, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	4	5	3	3	3	6	2	2	2	3	3	2
Mesh[T]	5	2	4	3	4	7	6	1	1	3	3	3
Mesh[T]Alt	2	2	1	1	2	3	2	1	1	1	2	1
Mesh[T]Chain	4	5	2	1	3	4	4	2	2	2	3	3
Mesh[T][S]	3	7	2	2	3	4	3	5	3	5	3	4
Mesh[T][S][FP]	3	2	2	2	2	4	4	3	2	3	3	2
Mesh[T][S]Sparse	7	20	4	4	6	8	7	6	4	5	6	4
Step[T]Alt	3	1	2	2	3	4	3	1	1	2	2	2
Step[T][S]	6	2	4	5	5	8	7	2	1	5	6	4
Step[T][S][FP]	6	2	5	5	6	9	7	2	1	4	5	4
Step[T][S][HP]	6	2	4	4	6	9	8	2	1	5	5	5
Step[T][S][HP]Async	6	2	5	4	6	9	7	2	1	5	5	5
Step[T][S][L]	11	5	8	8	12	16	12	4	3	9	10	8
Step[T][S][L]Cache	12	5	8	8	10	18	13	4	2	8	9	10
Step[T][S]Sparse	8	2	5	5	5	9	6	2	2	4	6	5
[T]Alt	2	2	1	1	2	3	2	1	1	1	1	1
[T][S]	3	8	2	2	3	4	3	5	4	4	2	4
[T][S][FP]	3	3	2	2	2	4	3	3	2	3	2	2
[T][S][HP]	2	3	2	2	2	4	3	3	2	3	3	2
[T][S][HP]Async	3	5	2	2	3	4	3	3	3	3	2	2
[T][S][L]	6	6	3	8	5	9	6	6	5	8	4	4
[T][S][L]Cache	6	7	4	4	4	6	7	6	7	6	4	4
[T][S]Sparse	6	16	4	5	5	10	7	6	4	6	5	4
sgd	5	6	3	3	4	7	5	2	2	4	4	3
step_sgd	3	6	2	2	3	4	4	3	2	3	3	2
step_tween	6	2	5	5	5	9	7	2	1	4	4	4
step_tween_chain	3	6	2	2	3	4	3	2	2	5	2	2
tween	5	2	3	4	5	8	5	2	1	3	3	3
tween_chain	4	3	3	3	2	5	5	2	2	3	2	3

Honesty - mean Score, every mode x dtype (cols 13-24)

Honesty - mean Score, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	4	5	3	3	5	2	2	3	7	3	5	3
Mesh[T]	2	3	1	2	2	1	1	4	4	2	2	2
Mesh[T]Alt	1	1	1	1	2	1	1	1	2	1	2	1
Mesh[T]Chain	4	5	3	4	5	2	1	3	7	3	5	3
Mesh[T][S]	6	5	3	6	7	4	3	4	10	5	9	5
Mesh[T][S][FP]	3	8	3	3	4	2	2	3	5	2	3	3
Mesh[T][S]Sparse	8	21	8	8	17	6	5	4	15	6	20	9
Step[T]Alt	2	1	1	1	1	0	1	2	2	1	1	1
Step[T][S]	4	4	2	3	3	1	1	5	5	2	3	3
Step[T][S][FP]	3	3	2	3	3	1	2	6	5	2	3	3
Step[T][S][HP]	4	3	1	3	3	1	2	6	5	2	1	3
Step[T][S][HP]Async	4	3	2	3	4	1	2	5	5	2	2	3
Step[T][S][L]	5	7	2	6	6	2	3	11	7	3	7	6
Step[T][S][L]Cache	6	6	3	6	8	2	3	9	10	3	6	6
Step[T][S]Sparse	3	3	1	3	3	1	2	5	5	2	3	3
[T]Alt	2	1	1	1	2	1	1	2	2	1	2	1
[T][S]	6	4	3	6	7	3	3	5	10	5	10	6
[T][S][FP]	3	8	3	4	4	2	2	2	6	2	3	3
[T][S][HP]	3	3	4	4	4	2	2	2	5	3	3	3
[T][S][HP]Async	6	7	4	5	7	3	3	2	8	5	5	5
[T][S][L]	11	17	7	11	20	5	6	5	20	8	7	10
[T][S][L]Cache	14	26	10	14	29	8	7	4	25	11	9	15
[T][S]Sparse	10	19	8	9	15	5	5	5	18	7	18	9
sgd	5	6	3	4	6	2	2	2	7	4	7	3
step_sgd	7	7	4	4	8	3	2	3	10	3	7	6
step_tween	3	4	2	4	3	1	1	6	6	2	4	3
step_tween_chain	4	7	3	5	6	3	2	2	6	3	7	5
tween	3	3	1	2	3	1	1	4	3	1	2	2
tween_chain	4	5	3	3	5	2	2	3	6	3	6	4

Honesty - mean Score, every mode x dtype (cols 25-34)

Honesty - mean Score, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	4	4	2	2	5	2	2	4	5	4
Mesh[T]	3	2	1	2	2	1	1	3	4	2
Mesh[T]Alt	2	1	1	2	1	1	1	1	2	1
Mesh[T]Chain	4	4	2	4	4	2	2	4	4	3
Mesh[T][S]	6	5	4	7	7	4	3	6	9	6
Mesh[T][S][FP]	3	4	3	4	3	2	2	4	5	3
Mesh[T][S]Sparse	9	12	7	10	10	6	5	9	17	8
Step[T]Alt	1	1	1	1	1	0	1	2	2	1
Step[T][S]	4	2	2	4	2	1	1	4	5	3
Step[T][S][FP]	4	2	1	4	2	1	2	3	5	3
Step[T][S][HP]	3	2	2	4	2	1	1	3	5	3
Step[T][S][HP]Async	4	2	1	4	2	1	2	3	6	3
Step[T][S][L]	7	3	3	6	5	2	3	6	10	7
Step[T][S][L]Cache	6	3	3	6	4	3	2	6	9	6
Step[T][S]Sparse	4	2	1	3	3	1	2	3	5	4
[T]Alt	1	1	1	1	1	1	1	1	2	1
[T][S]	6	6	5	6	7	4	3	6	9	6
[T][S][FP]	3	2	3	4	4	2	2	4	5	3
[T][S][HP]	4	3	2	3	4	2	2	4	4	3
[T][S][HP]Async	6	4	4	6	5	3	3	5	8	5
[T][S][L]	11	5	7	13	12	6	5	12	17	10
[T][S][L]Cache	17	4	11	17	16	8	8	15	25	13
[T][S]Sparse	11	10	7	12	11	5	5	9	16	7
sgd	4	4	3	5	5	2	2	4	7	4
step_sgd	6	5	4	5	5	3	2	5	7	5
step_tween	3	3	2	4	3	1	1	4	6	2
step_tween_chain	6	5	3	5	5	3	3	5	6	4
tween	3	2	1	3	2	1	1	3	5	2
tween_chain	4	4	3	4	4	1	2	4	7	4

Honesty - mean hard Acc, every mode x dtype (cols 1-12)

Honesty - mean hard Acc, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	5	7	5	5	5	6	3	3	6	5	5	3
Mesh[T]	9	3	10	8	9	10	10	2	4	8	7	7
Mesh[T]Alt	3	7	3	3	3	3	3	3	5	5	3	4
Mesh[T]Chain	6	7	5	3	6	4	5	3	6	3	5	5
Mesh[T][S]	3	6	3	2	3	3	3	5	7	5	3	5
Mesh[T][S][FP]	3	2	3	3	3	3	3	3	4	3	3	3
Mesh[T][S]Sparse	3	7	3	3	3	3	3	2	5	2	3	3
Step[T]Alt	9	3	8	9	10	9	7	3	4	7	8	10
Step[T][S]	8	2	8	9	8	8	8	3	4	9	9	8
Step[T][S][FP]	8	2	10	8	10	9	9	3	4	7	9	7
Step[T][S][HP]	9	3	8	8	9	9	10	3	4	9	9	10
Step[T][S][HP]Async	8	3	9	8	9	9	8	3	4	8	7	9
Step[T][S][L]	7	3	9	9	10	8	8	3	5	9	9	9
Step[T][S][L]Cache	8	3	9	9	8	9	9	3	4	8	8	10
Step[T][S]Sparse	10	2	9	8	8	9	8	3	5	7	8	9
[T]Alt	3	7	2	3	3	3	2	4	6	5	3	5
[T][S]	3	7	2	2	3	3	3	5	7	5	2	5
[T][S][FP]	3	2	3	3	2	3	3	3	4	3	3	3
[T][S][HP]	2	3	3	2	2	3	3	3	4	3	3	2
[T][S][HP]Async	3	5	2	3	3	3	3	3	6	3	3	3
[T][S][L]	3	3	2	6	3	3	2	3	6	5	2	3
[T][S][L]Cache	3	3	3	3	2	2	3	3	8	3	2	3
[T][S]Sparse	2	6	3	3	3	3	3	3	5	3	2	3
sgd	5	7	5	5	5	5	5	3	6	5	6	5
step_sgd	3	5	3	3	3	2	3	3	4	3	3	3
step_tween	8	3	9	9	9	8	8	3	4	8	7	8
step_tween_chain	2	6	3	3	3	3	3	2	5	6	3	3
tween	9	3	8	9	10	9	9	3	5	7	7	9
tween_chain	5	3	5	6	3	5	6	3	7	5	3	6

Honesty - mean hard Acc, every mode x dtype (cols 13-24)

Honesty - mean hard Acc, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	7	7	7	6	6	5	6	5	7	7	7	6
Mesh[T]	6	5	5	5	4	4	4	9	6	5	4	6
Mesh[T]Alt	6	5	5	6	6	6	6	4	6	5	6	6
Mesh[T]Chain	6	7	7	7	6	7	5	6	7	6	6	6
Mesh[T][S]	7	5	6	7	7	7	7	5	7	7	8	6
Mesh[T][S][FP]	4	7	5	4	4	4	4	3	4	3	2	4
Mesh[T][S]Sparse	5	7	6	5	6	6	6	3	5	4	7	5
Step[T]Alt	7	4	4	5	4	3	4	9	5	3	3	5
Step[T][S]	6	4	4	5	4	3	5	9	5	4	3	5
Step[T][S][FP]	5	4	4	6	4	4	5	10	6	4	4	5
Step[T][S][HP]	6	4	4	6	4	4	5	9	5	4	2	6
Step[T][S][HP]Async	6	4	4	6	4	4	5	9	6	4	3	5
Step[T][S][L]	5	4	4	6	3	4	5	11	4	4	4	6
Step[T][S][L]Cache	6	3	4	6	4	3	5	9	5	3	4	6
Step[T][S]Sparse	5	4	3	6	4	4	5	9	5	4	3	5
[T]Alt	7	4	6	7	6	6	5	5	6	6	6	5
[T][S]	7	4	5	7	6	7	7	5	7	7	8	7
[T][S][FP]	4	7	5	4	3	4	4	3	5	3	3	4
[T][S][HP]	4	3	6	5	4	5	4	2	4	4	2	4
[T][S][HP]Async	7	7	7	6	6	6	7	2	6	6	5	6
[T][S][L]	7	7	7	7	7	7	7	3	8	7	3	7
[T][S][L]Cache	8	9	8	8	9	8	8	3	8	8	3	9
[T][S]Sparse	6	7	6	5	5	5	6	3	6	5	6	5
sgd	7	6	7	6	6	6	7	3	6	7	7	4
step_sgd	7	6	6	4	7	5	5	3	7	5	6	6
step_tween	5	5	4	6	4	4	4	9	6	5	5	5
step_tween_chain	5	7	6	6	6	6	5	2	5	4	7	7
tween	6	6	5	5	5	4	5	10	4	4	4	6
tween_chain	6	7	6	5	6	6	6	5	6	7	7	7

Honesty - mean hard Acc, every mode x dtype (cols 25-34)

Honesty - mean hard Acc, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	6	7	4	4	8	7	7	7	6	7
Mesh[T]	6	5	5	5	5	4	5	7	6	5
Mesh[T]Alt	7	5	6	7	5	7	5	6	6	6
Mesh[T]Chain	6	6	5	7	7	6	7	6	4	5
Mesh[T][S]	7	6	7	7	8	7	7	7	7	7
Mesh[T][S][FP]	4	4	4	5	4	4	4	4	4	4
Mesh[T][S]Sparse	5	6	6	5	5	6	5	5	6	5
Step[T]Alt	5	3	3	5	3	3	4	5	6	5
Step[T][S]	6	3	4	6	4	4	4	6	5	5
Step[T][S][FP]	5	4	3	6	3	3	5	5	6	6
Step[T][S][HP]	6	3	4	6	3	4	5	6	6	6
Step[T][S][HP]Async	6	4	3	5	4	4	6	5	6	5
Step[T][S][L]	6	3	4	5	4	4	5	5	6	6
Step[T][S][L]Cache	5	3	4	5	4	4	4	5	5	6
Step[T][S]Sparse	5	4	3	5	4	4	5	5	5	6
[T]Alt	6	6	6	5	6	7	6	6	5	6
[T][S]	7	7	8	7	7	7	7	7	7	7
[T][S][FP]	4	3	4	4	4	4	4	4	4	4
[T][S][HP]	4	3	4	4	4	4	4	4	3	4
[T][S][HP]Async	6	5	6	7	6	6	6	6	7	6
[T][S][L]	6	3	7	7	7	7	7	7	7	7
[T][S][L]Cache	8	2	9	9	8	8	8	8	9	8
[T][S]Sparse	6	6	5	6	6	5	5	5	5	5
sgd	6	6	7	7	7	7	7	6	6	6
step_sgd	6	6	7	6	5	6	5	5	5	6
step_tween	5	5	4	6	4	4	4	5	6	4
step_tween_chain	6	6	6	5	6	6	6	6	5	5
tween	6	5	4	6	3	4	5	6	6	5
tween_chain	6	7	6	7	7	4	7	7	7	7

Honesty - mean SoftAcc, every mode x dtype (cols 1-12)

Honesty - mean SoftAcc, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	5	4	5	5	5	6	0	2	4	5	5	2
Mesh[T]	2	2	2	2	2	2	2	2	2	2	2	2
Mesh[T]Alt	0	6	0	0	0	0	0	3	5	5	0	4
Mesh[T]Chain	6	5	5	1	6	3	5	2	4	2	5	5
Mesh[T][S]	0	2	0	0	0	0	0	5	4	5	0	5
Mesh[T][S][FP]	0	2	0	0	0	0	0	2	2	2	0	2
Mesh[T][S]Sparse	0	4	0	0	0	0	0	2	4	2	0	2
Step[T]Alt	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S]	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][FP]	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][HP]	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][HP]Async	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][L]	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][L]Cache	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S]Sparse	2	2	2	2	2	2	2	2	2	2	2	2
[T]Alt	0	6	0	0	0	0	0	4	5	5	0	5
[T][S]	0	2	0	0	0	0	0	5	5	5	0	5
[T][S][FP]	0	2	0	0	0	0	0	2	2	2	0	2
[T][S][HP]	0	2	0	0	0	0	0	2	3	2	0	2
[T][S][HP]Async	0	2	0	0	0	0	0	2	4	2	0	2
[T][S][L]	0	2	0	5	0	0	0	2	4	5	0	2
[T][S][L]Cache	0	2	0	0	0	0	0	2	5	3	0	2
[T][S]Sparse	0	4	0	0	0	0	0	2	3	2	0	2
sgd	5	4	5	5	5	5	5	2	4	5	6	5
step_sgd	0	3	0	0	0	0	0	2	3	2	0	2
step_tween	2	2	2	2	2	2	2	2	2	2	2	2
step_tween_chain	0	4	0	0	0	0	0	2	4	6	0	2
tween	2	2	2	2	2	2	2	2	2	2	2	2
tween_chain	5	2	5	6	1	5	6	2	5	5	0	6

Honesty - mean SoftAcc, every mode x dtype (cols 13-24)

Honesty - mean SoftAcc, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	4	4	4	4	4	3	4	5	4	4	4	4
Mesh[T]	2	2	2	2	2	2	2	2	2	2	2	2
Mesh[T]Alt	5	4	5	5	5	5	5	4	5	5	5	5
Mesh[T]Chain	4	5	4	5	4	4	3	6	4	4	4	4
Mesh[T][S]	5	4	4	5	4	5	5	5	5	4	4	5
Mesh[T][S][FP]	2	4	4	2	2	2	3	2	2	3	2	2
Mesh[T][S]Sparse	3	4	4	4	4	4	4	2	4	3	4	4
Step[T]Alt	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S]	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][FP]	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][HP]	2	2	2	2	2	2	2	2	2	2	1	2
Step[T][S][HP]Async	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][L]	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S][L]Cache	2	2	2	2	2	2	2	2	2	2	2	2
Step[T][S]Sparse	2	2	2	2	2	2	2	2	2	2	2	2
[T]Alt	6	4	5	6	5	5	5	5	6	6	5	5
[T][S]	5	4	4	5	4	4	4	5	4	4	4	5
[T][S][FP]	3	4	4	2	3	3	3	2	2	2	2	2
[T][S][HP]	2	2	4	3	3	2	2	2	2	2	2	2
[T][S][HP]Async	5	5	4	4	3	4	4	2	4	4	3	3
[T][S][L]	5	4	4	5	5	4	5	2	5	4	2	5
[T][S][L]Cache	5	4	4	5	5	5	5	2	5	5	2	5
[T][S]Sparse	4	4	4	4	4	4	4	2	4	3	4	3
sgd	4	4	4	4	4	4	4	2	4	4	4	3
step_sgd	4	4	4	3	4	4	4	2	4	3	4	4
step_tween	2	2	2	2	2	2	2	2	2	2	2	2
step_tween_chain	3	4	4	4	4	4	3	2	3	3	4	4
tween	2	2	2	2	2	2	2	2	2	2	2	2
tween_chain	4	4	4	4	4	5	4	5	4	4	5	4

Honesty - mean SoftAcc, every mode x dtype (cols 25-34)

Honesty - mean SoftAcc, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	4	4	3	3	5	4	4	4	4	4
Mesh[T]	2	2	2	2	2	2	2	2	2	2
Mesh[T]Alt	6	5	5	6	5	6	5	5	5	5
Mesh[T]Chain	4	4	4	4	5	4	4	4	3	4
Mesh[T][S]	5	4	4	5	4	5	4	5	5	5
Mesh[T][S][FP]	3	3	3	3	2	3	2	3	3	3
Mesh[T][S]Sparse	4	4	4	4	4	4	3	3	4	3
Step[T]Alt	2	2	2	2	2	2	2	2	2	2
Step[T][S]	2	2	2	2	2	2	2	2	2	2
Step[T][S][FP]	2	2	2	2	2	2	2	2	2	2
Step[T][S][HP]	2	2	2	2	2	2	2	2	2	2
Step[T][S][HP]Async	2	2	2	2	2	2	2	2	2	2
Step[T][S][L]	2	2	2	2	2	2	2	2	2	2
Step[T][S][L]Cache	2	2	2	2	2	2	2	2	2	2
Step[T][S]Sparse	2	2	2	2	2	2	2	2	2	2
[T]Alt	5	5	5	5	5	6	5	5	5	6
[T][S]	5	4	5	5	4	4	4	5	4	5
[T][S][FP]	2	2	2	2	3	2	2	2	2	2
[T][S][HP]	2	2	2	2	3	2	2	3	2	2
[T][S][HP]Async	4	3	4	4	4	4	4	4	4	3
[T][S][L]	4	2	4	5	4	5	5	4	5	4
[T][S][L]Cache	5	2	4	5	5	5	5	4	5	5
[T][S]Sparse	4	4	4	4	4	4	4	4	4	3
sgd	4	4	4	4	4	4	4	4	4	4
step_sgd	4	4	4	4	3	4	3	3	3	4
step_tween	2	2	2	2	2	2	2	2	2	2
step_tween_chain	4	4	4	4	4	4	4	4	3	3
tween	2	2	2	2	2	2	2	2	2	2
tween_chain	4	4	4	4	4	3	4	4	4	5

Honesty - mean Avail, every mode x dtype (cols 1-12)

Honesty - mean Avail, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	23	21	24	24	23	23	24	22	24	23	23	24
Mesh[T]	20	18	21	21	21	20	21	20	21	21	21	21
Mesh[T]Alt	23	13	23	23	23	23	22	14	16	16	23	18
Mesh[T]Chain	23	21	24	24	23	23	23	22	24	23	24	24
Mesh[T][S]	26	25	28	28	27	26	28	26	29	28	27	29
Mesh[T][S][FP]	27	24	29	29	27	27	28	26	29	28	28	29
Mesh[T][S]Sparse	36	36	36	37	37	36	36	36	37	36	36	36
Step[T]Alt	16	14	17	17	17	17	18	16	17	17	17	17
Step[T][S]	24	22	24	25	24	23	25	22	25	25	24	25
Step[T][S][FP]	23	21	25	25	23	23	24	23	25	25	23	25
Step[T][S][HP]	22	21	24	24	23	23	24	22	24	24	23	24
Step[T][S][HP]Async	23	22	25	25	24	23	24	23	24	25	24	25
Step[T][S][L]	31	30	30	30	31	30	30	29	30	31	30	30
Step[T][S][L]Cache	30	30	31	30	31	30	31	29	30	31	30	31
Step[T][S]Sparse	23	21	25	25	24	23	24	23	25	25	24	24
[T]Alt	23	13	23	23	23	23	23	14	16	16	23	19
[T][S]	26	25	28	29	28	26	28	26	29	28	28	28
[T][S][FP]	26	25	29	29	27	26	28	26	29	28	28	28
[T][S][HP]	26	25	29	28	28	26	28	26	29	28	27	29
[T][S][HP]Async	26	25	28	29	27	26	28	26	29	28	27	28
[T][S][L]	34	31	36	36	35	36	36	35	35	35	36	37
[T][S][L]Cache	35	35	36	36	35	36	36	36	37	37	36	37
[T][S]Sparse	36	35	36	36	36	36	36	35	37	37	36	36
sgd	23	21	25	24	24	24	24	23	24	24	24	24
step_sgd	26	24	28	28	27	27	28	26	28	28	27	28
step_tween	23	20	24	24	24	23	24	22	24	24	23	24
step_tween_chain	26	23	28	26	27	26	27	25	28	27	27	28
tween	21	18	21	22	21	21	21	20	21	21	21	21
tween_chain	23	21	24	24	23	23	24	22	24	24	24	24

Honesty - mean Avail, every mode x dtype (cols 13-24)

Honesty - mean Avail, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	24	20	24	24	21	24	24	24	23	24	21	23
Mesh[T]	21	19	21	22	19	21	21	22	20	20	18	21
Mesh[T]Alt	16	13	16	16	14	16	16	18	14	16	13	16
Mesh[T]Chain	24	20	24	25	21	24	24	24	23	23	21	23
Mesh[T][S]	29	24	28	29	24	28	29	29	26	28	24	28
Mesh[T][S][FP]	29	25	29	29	25	29	29	29	25	28	24	28
Mesh[T][S]Sparse	36	35	37	36	36	37	37	37	35	36	35	36
Step[T]Alt	18	14	17	17	15	18	17	18	16	17	13	17
Step[T][S]	25	21	25	25	22	25	25	25	23	24	22	24
Step[T][S][FP]	25	21	24	25	21	24	25	25	22	24	21	24
Step[T][S][HP]	24	20	24	24	21	24	24	25	22	24	18	23
Step[T][S][HP]Async	25	21	24	25	22	24	25	25	22	24	21	24
Step[T][S][L]	31	29	30	31	30	30	30	30	30	30	29	30
Step[T][S][L]Cache	31	29	30	30	30	30	30	31	30	30	29	30
Step[T][S]Sparse	25	21	25	25	22	25	25	25	22	25	21	24
[T]Alt	16	13	16	16	13	16	16	19	15	16	13	15
[T][S]	29	24	29	29	24	29	29	29	26	28	25	28
[T][S][FP]	28	24	29	29	25	29	29	29	26	28	23	28
[T][S][HP]	28	24	29	29	24	29	28	30	26	29	24	28
[T][S][HP]Async	28	24	29	29	25	29	29	29	26	28	24	28
[T][S][L]	35	33	35	36	34	35	35	37	34	35	31	35
[T][S][L]Cache	37	35	37	37	36	37	37	37	36	36	35	37
[T][S]Sparse	36	35	37	36	35	37	37	37	35	37	35	36
sgd	25	21	25	25	22	24	24	24	23	24	22	24
step_sgd	28	23	28	29	24	28	28	29	26	27	24	28
step_tween	24	20	24	24	20	24	24	25	22	24	20	23
step_tween_chain	28	23	28	28	24	28	28	28	26	28	23	27
tween	22	18	21	22	19	21	21	22	20	21	17	21
tween_chain	25	21	25	25	22	24	24	24	22	24	21	24

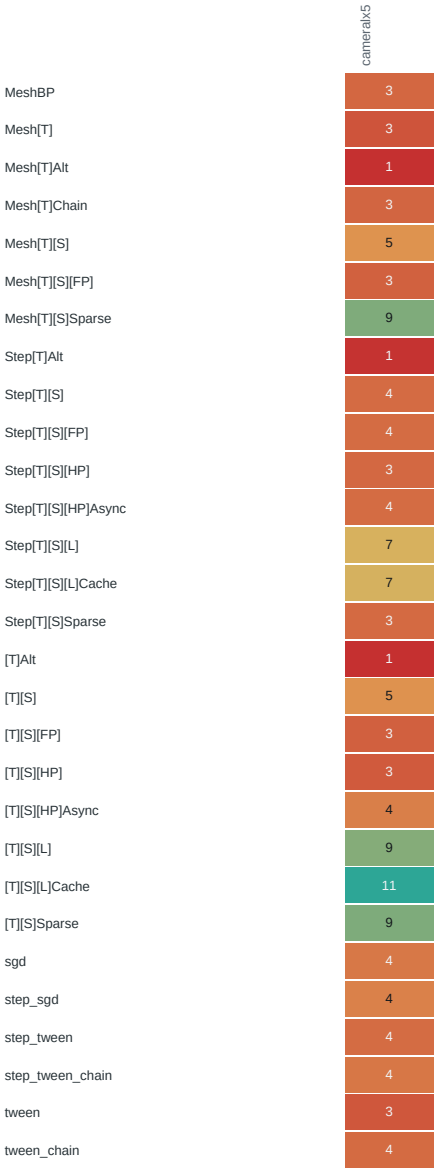
Honesty - mean Avail, every mode x dtype (cols 25-34)

Honesty - mean Avail, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	23	24	24	23	23	23	24	23	23	24
Mesh[T]	21	21	21	21	21	21	21	21	20	21
Mesh[T]Alt	15	15	16	15	16	16	16	15	15	16
Mesh[T]Chain	23	23	23	23	23	23	24	23	23	24
Mesh[T][S]	27	27	28	28	28	29	29	27	27	28
Mesh[T][S][FP]	28	27	29	28	28	29	29	28	27	28
Mesh[T][S]Sparse	36	37	36	36	36	37	37	36	37	36
Step[T]Alt	17	16	17	17	17	17	17	17	16	17
Step[T][S]	24	24	24	24	24	24	25	24	24	24
Step[T][S][FP]	24	24	24	24	24	25	24	24	23	24
Step[T][S][HP]	23	24	24	24	23	24	23	23	23	24
Step[T][S][HP]Async	24	24	24	24	24	24	24	24	23	24
Step[T][S][L]	30	30	30	30	31	30	30	30	30	31
Step[T][S][L]Cache	30	30	30	30	30	30	30	31	30	31
Step[T][S]Sparse	24	24	24	24	24	24	24	24	23	24
[T]Alt	15	15	16	16	15	16	16	16	15	16
[T][S]	28	28	28	28	28	29	28	28	27	28
[T][S][FP]	28	27	28	28	28	28	29	28	27	28
[T][S][HP]	28	28	29	28	28	29	29	28	26	28
[T][S][HP]Async	27	27	28	28	28	29	29	27	27	28
[T][S][L]	35	35	34	36	35	35	35	36	34	35
[T][S][L]Cache	37	36	37	37	37	37	37	37	36	37
[T][S]Sparse	37	36	37	36	36	37	37	36	36	36
sgd	24	24	25	24	24	24	24	24	24	25
step_sgd	28	27	28	27	27	28	28	27	27	28
step_tween	24	23	23	24	24	24	24	24	23	24
step_tween_chain	27	27	27	27	27	27	27	27	27	27
tween	21	21	21	21	21	21	21	21	21	21
tween_chain	24	23	24	24	24	24	24	24	24	24

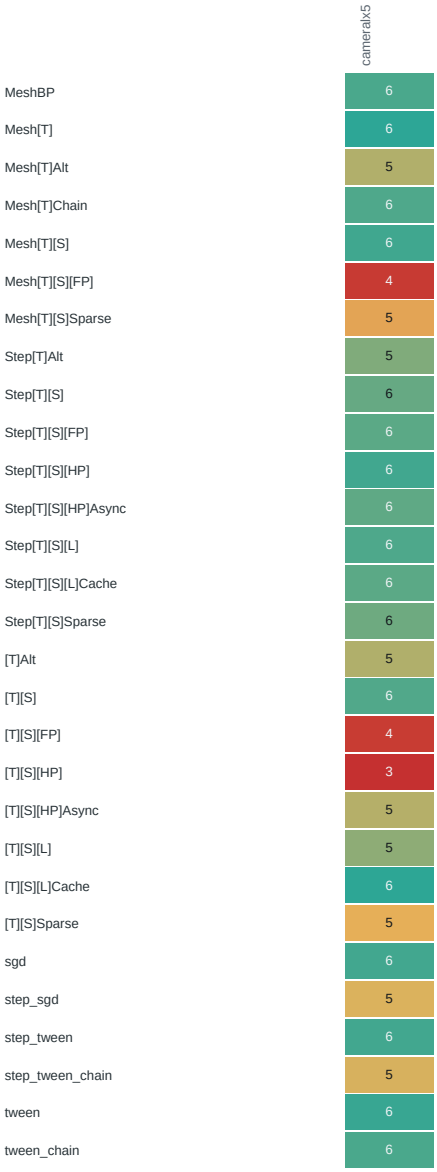
Mean Score, every mode x arch

Mean Score, every mode x arch



Mean hard Acc, every mode x arch

Mean hard Acc, every mode x arch

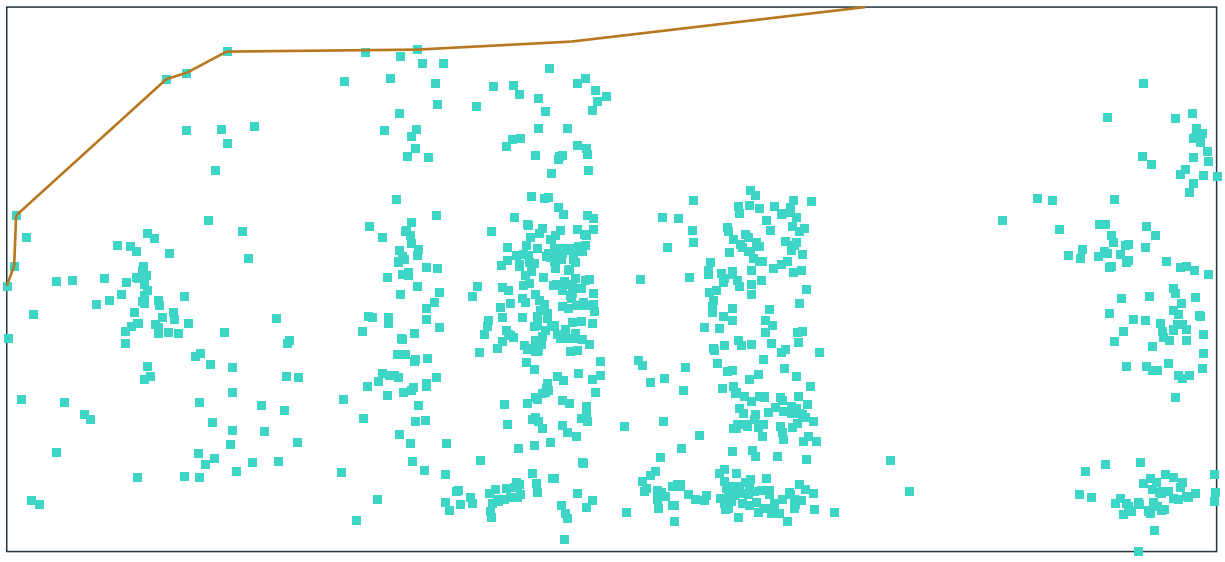


Mean Avail, every mode x arch

Mean Avail, every mode x arch

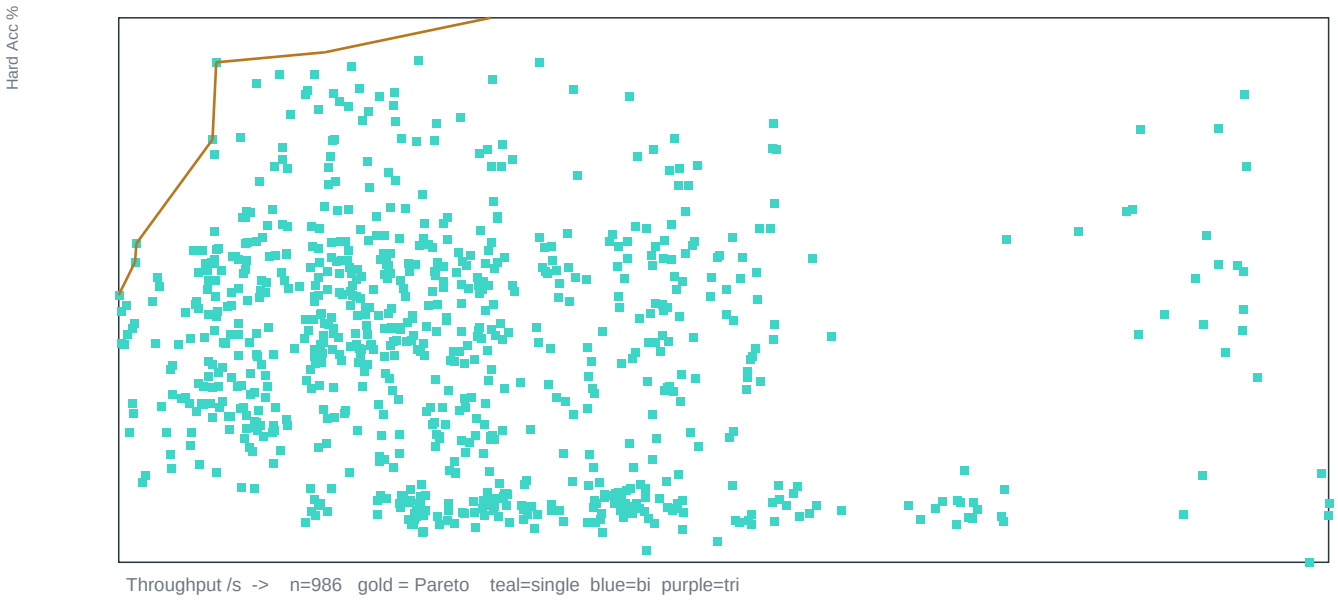
	cameralx5
MeshBP	23
Mesh[T]	20
Mesh[T]Alt	17
Mesh[T]Chain	23
Mesh[T][S]	27
Mesh[T][S][FP]	28
Mesh[T][S]Sparse	36
Step[T]Alt	17
Step[T][S]	24
Step[T][S][FP]	24
Step[T][S][HP]	23
Step[T][S][HP]Async	24
Step[T][S][L]	30
Step[T][S][L]Cache	30
Step[T][S]Sparse	24
[T]Alt	17
[T][S]	27
[T][S][FP]	27
[T][S][HP]	27
[T][S][HP]Async	27
[T][S][L]	35
[T][S][L]Cache	36
[T][S]Sparse	36
sgd	24
step_sgd	27
step_tween	23
step_tween_chain	27
tween	21
tween_chain	23

Pillars - Availability vs hard Acc

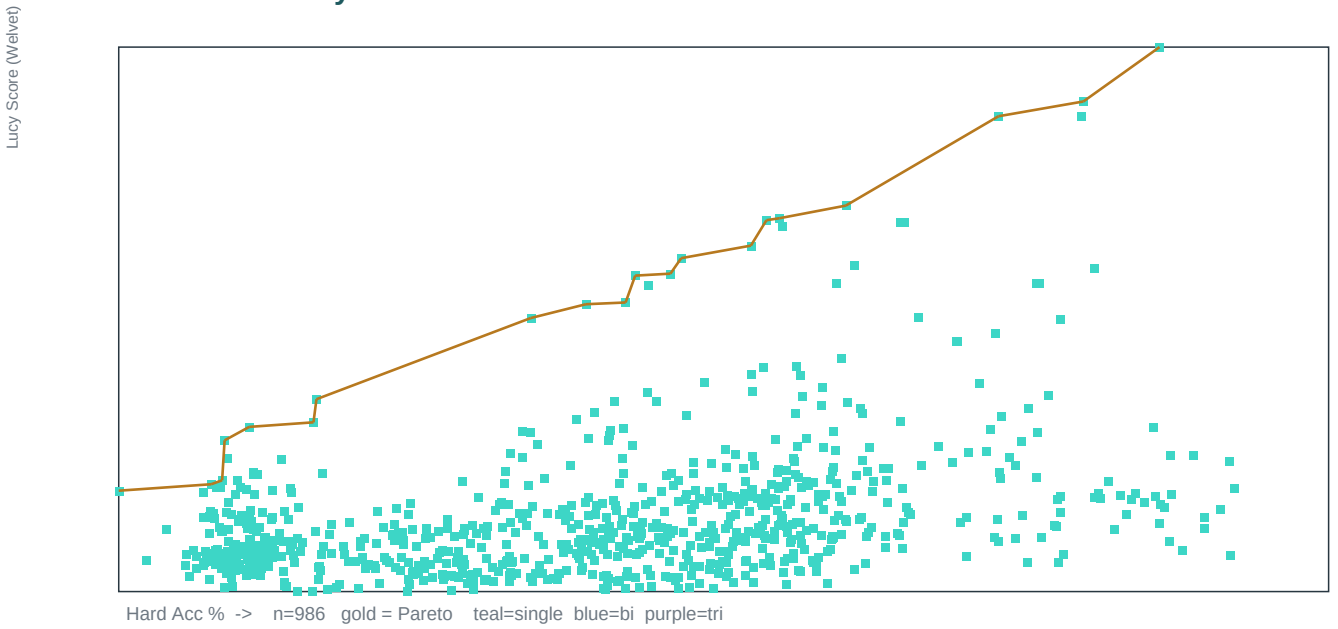



Availability % -> n=986 gold = Pareto teal=single blue=bi purple=tri
Hard Acc %

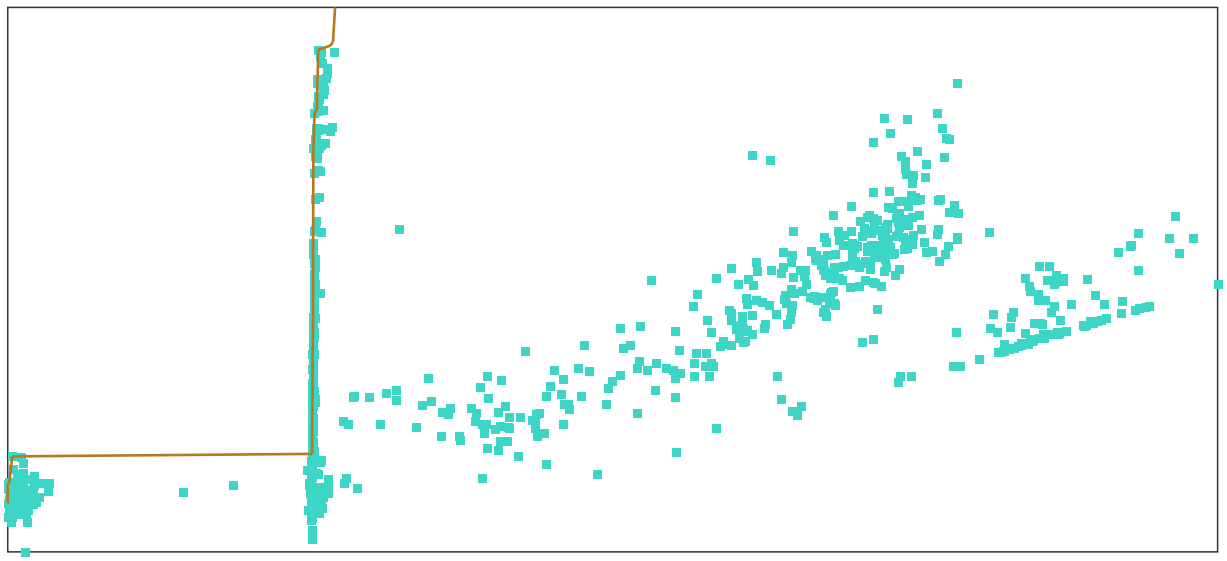
Pillars - Throughput vs hard Acc



Pareto - hard Acc vs Lucy Score

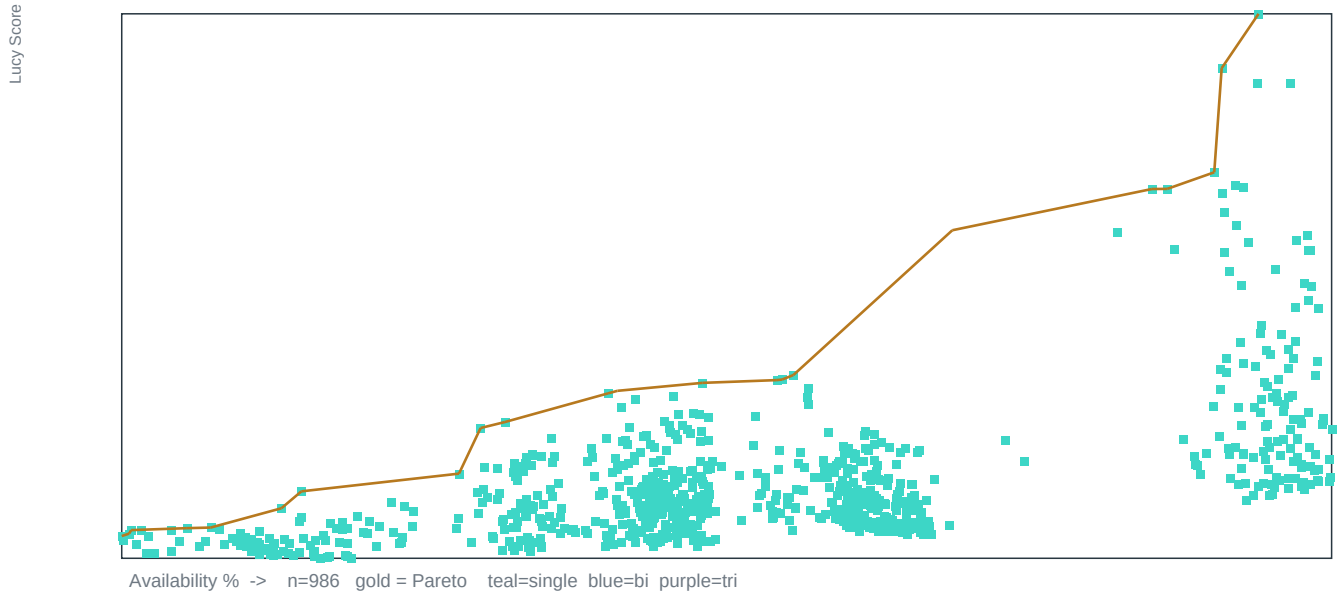


SoftAcc (serve-confidence) vs hard Acc




SoftAcc % -> n=986 gold = Pareto teal=single blue=bi purple=tri
Hard Acc %

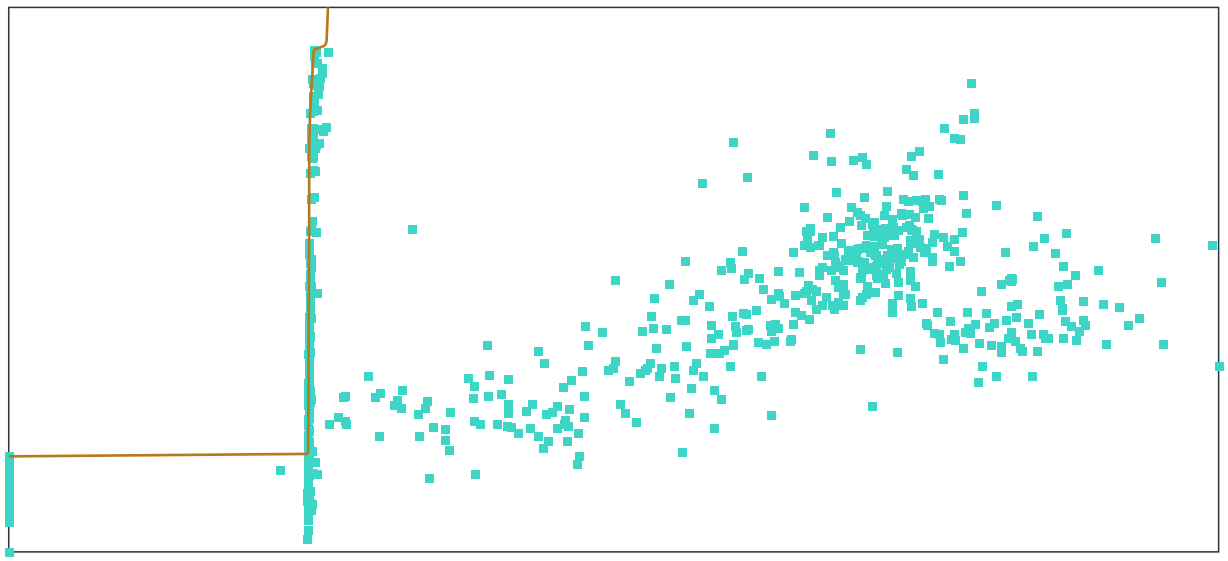
Avail vs Lucy Score (duty clock)



Pillars - Throughput vs Availability



AdaptPct vs hard Acc



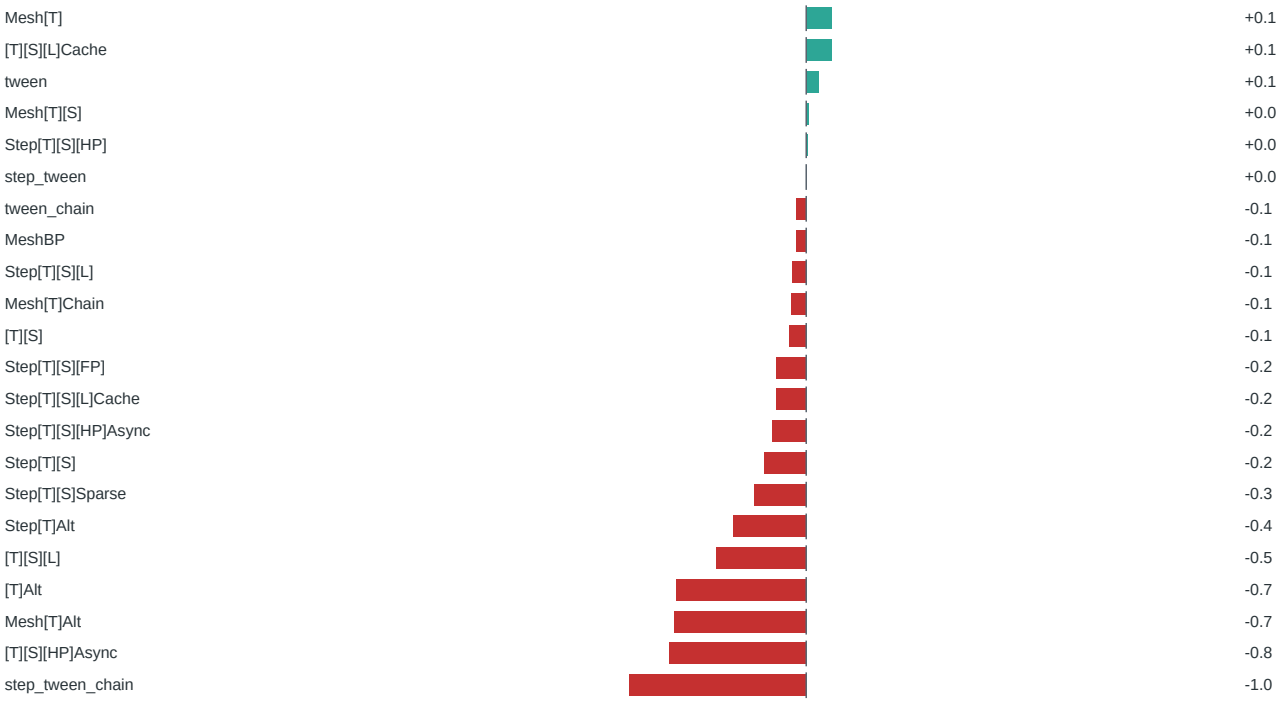

AdaptPct % -> n=986 gold = Pareto teal=single blue=bi purple=tri
Hard Acc %

vs sgd - matched dtype x format x arch

AccDelta is the honest column. ScoreDelta is usually Availability (duty clock), not a better chain rule. Acc win = AccDelta > 0.5. Score win = ScoreDelta > 1. Baseline is discovered from the board, not a frozen StepBP list.

mode	n	AccD	Acc win%	SoftD	AvailD	ThruD	ScoreD	Score win%
Mesh[T]	34	+0.1	35	-2.7	-3.2	-80	-1.3	6
[T][S][L]Cache	34	+0.1	59	-1.2	+12.6	+230	+6.9	85
tween	34	+0.1	32	-2.7	-3.0	-70	-1.2	6
Mesh[T][S]	34	+0.0	56	-0.7	+3.6	+28	+1.0	68
Step[T][S][HP]	34	+0.0	32	-2.7	-0.7	-49	-0.6	29
step_tween	34	+0.0	32	-2.7	-0.5	-39	-0.5	24
tween_chain	34	-0.1	24	-0.1	-0.2	-32	-0.5	6
MeshBP	34	-0.1	24	-0.2	-0.6	-40	-0.6	3
Step[T][S][L]	34	-0.1	35	-2.7	+6.4	+90	+2.5	53
Mesh[T]Chain	34	-0.1	24	-0.1	-0.6	-42	-0.7	3
[T][S]	34	-0.1	38	-0.7	+3.8	+30	+1.0	68
Step[T][S][FP]	34	-0.2	29	-2.7	-0.1	-34	-0.5	24
Step[T][S][L]Cache	34	-0.2	35	-2.7	+6.4	+90	+2.6	62
Step[T][S][HP]Async	34	-0.2	32	-2.7	+0.0	-30	-0.4	26
Step[T][S]	34	-0.2	35	-2.7	+0.1	-32	-0.5	26
Step[T][S]Sparse	34	-0.3	35	-2.7	+0.0	-31	-0.5	26
Step[T]Alt	34	-0.4	32	-2.7	-7.2	-135	-2.5	0
[T][S][L]	34	-0.5	29	-1.1	+11.2	+192	+4.6	82
[T]Alt	34	-0.7	15	-0.1	-6.8	-121	-2.7	0
Mesh[T]Alt	34	-0.7	15	-0.2	-6.8	-122	-2.7	0
[T][S][HP]Async	34	-0.8	6	-1.5	+3.7	+27	+0.3	41
step_tween_chain	34	-1.0	9	-1.4	+3.0	+22	-0.1	15
step_sgd	34	-1.0	12	-1.5	+3.4	+47	+0.3	24
[T][S]Sparse	34	-1.1	3	-1.5	+12.4	+231	+4.8	97
Mesh[T][S]Sparse	34	-1.2	9	-1.5	+12.5	+237	+4.8	94
[T][S][FP]	34	-2.2	3	-2.5	+3.8	+28	-0.9	3
Mesh[T][S][FP]	34	-2.2	6	-2.4	+3.9	+33	-0.9	6
[T][S][HP]	34	-2.3	0	-2.5	+3.8	+23	-1.1	0

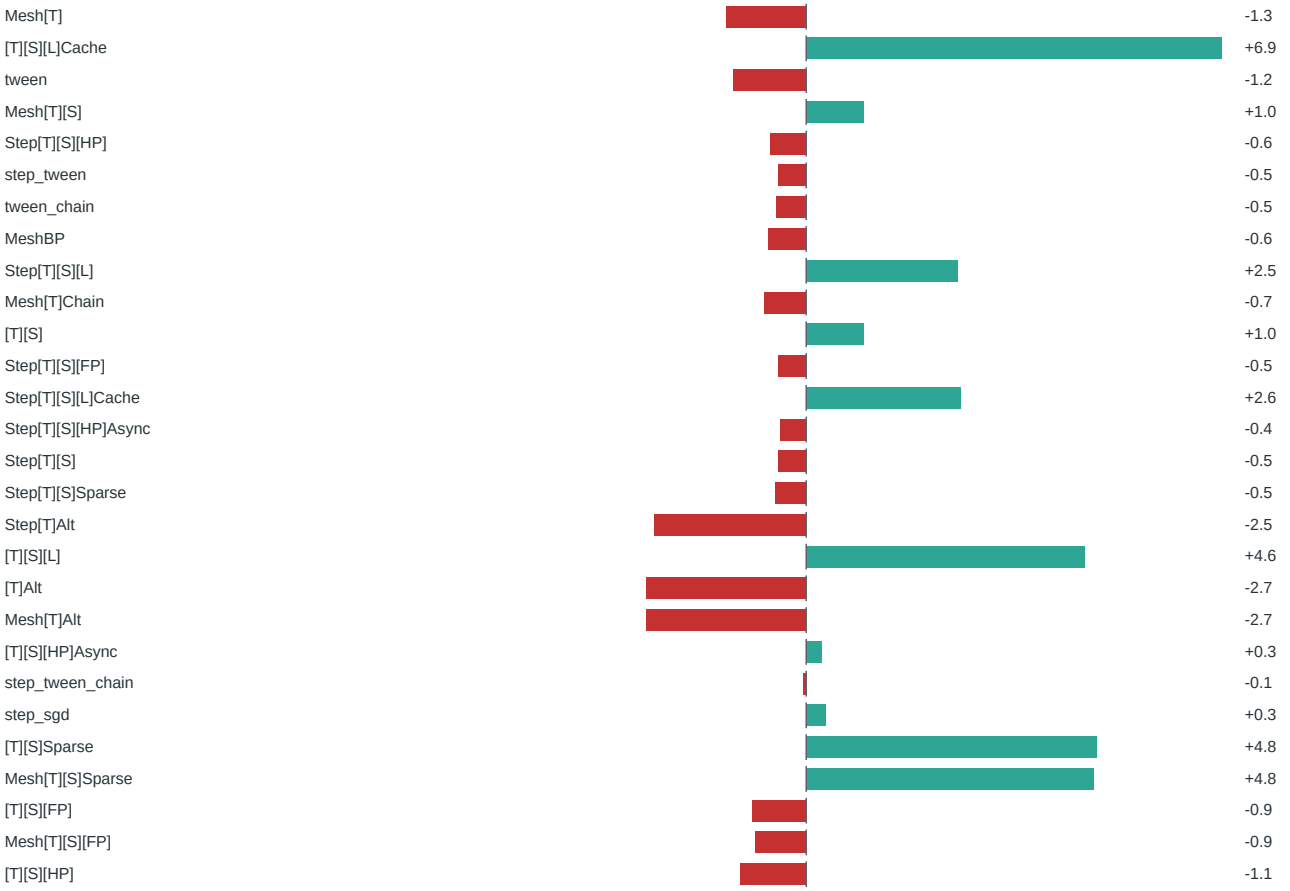
mean AccD vs sgd



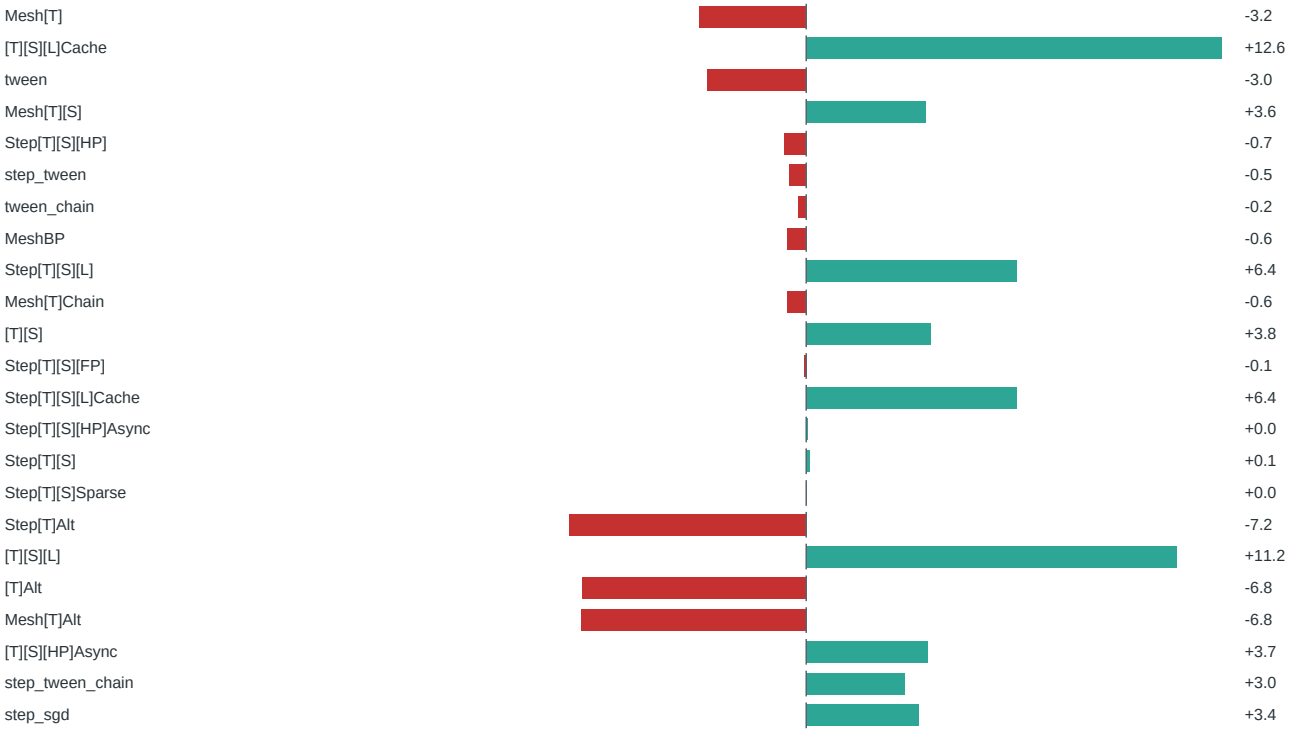
mean AccD vs sgd



mean ScoreD vs sgd (duty clock)



mean AvailD vs sgd



mean AvailD vs sgd



AccD vs sgd, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	+0	-0	+0	-0	+0	+0	-2	-0	+0	+0	-1	-2
Mesh[T]	+4	-3	+5	+3	+3	+4	+5	-0	-2	+3	+1	+2
Mesh[T]Alt	-3	+1	-2	-2	-2	-3	-2	+1	-1	-0	-3	-1
Mesh[T]Chain	+0	+0	-0	-2	+0	-1	+0	+0	-0	-2	-1	+0
Mesh[T][S]	-2	-1	-3	-3	-2	-3	-2	+2	+1	-0	-3	+0
Mesh[T][S][FP]	-3	-5	-3	-2	-3	-3	-2	+0	-3	-3	-3	-3
Mesh[T][S]Sparse	-2	-0	-2	-2	-3	-3	-2	-0	-2	-3	-3	-3
Step[T]Alt	+4	-4	+3	+4	+4	+3	+2	+0	-2	+2	+2	+5
Step[T][S]	+3	-4	+3	+4	+2	+3	+3	+1	-2	+4	+3	+3
Step[T][S][FP]	+3	-4	+5	+3	+5	+4	+4	+0	-2	+2	+3	+2
Step[T][S][HP]	+4	-4	+3	+3	+4	+4	+5	-0	-2	+3	+4	+5
Step[T][S][HP]Async	+3	-4	+4	+3	+4	+3	+3	+0	-2	+3	+1	+4
Step[T][S][L]	+2	-4	+4	+4	+5	+3	+3	-0	-1	+4	+3	+3
Step[T][S][L]Cache	+3	-4	+3	+4	+3	+4	+3	-0	-2	+2	+2	+5
Step[T][S]Sparse	+5	-4	+4	+3	+2	+3	+3	+0	-1	+1	+3	+3
[T]Alt	-2	+0	-3	-2	-3	-3	-3	+1	-0	-1	-3	-1
[T][S]	-2	+0	-3	-3	-3	-3	-2	+2	+1	-0	-3	+0
[T][S][FP]	-3	-4	-2	-2	-3	-3	-2	+0	-2	-2	-3	-2
[T][S][HP]	-3	-4	-2	-3	-3	-3	-2	-0	-2	-3	-3	-3
[T][S][HP]Async	-2	-2	-3	-2	-3	-3	-2	+0	-0	-2	-3	-2
[T][S][L]	-3	-4	-3	+1	-3	-3	-3	-0	+0	+0	-3	-3
[T][S][L]Cache	-3	-4	-3	-2	-3	-4	-2	-0	+2	-2	-3	-3
[T][S]Sparse	-3	-1	-2	-2	-3	-2	-2	-0	-1	-2	-3	-3
step_sgd	-2	-1	-2	-2	-3	-3	-2	+0	-2	-3	-3	-3
step_tween	+3	-4	+4	+4	+3	+3	+3	-0	-2	+3	+1	+3
step_tween_chain	-3	-1	-2	-2	-3	-2	-2	-0	-1	+1	-3	-2
tween	+4	-3	+3	+4	+5	+4	+4	-0	-1	+2	+1	+3
tween_chain	+0	-3	+0	+1	-2	-0	+0	+0	+0	-0	-3	+1

AccD vs sgd, every mode x dtype (cols 13-24)

AccD vs sgd, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	+0	+1	+1	+0	+0	-1	-1	+3	+1	+0	-1	+2
Mesh[T]	-1	-1	-2	-0	-2	-1	-2	+7	-0	-2	-4	+2
Mesh[T]Alt	-1	-1	-1	-0	+0	-0	-1	+1	+0	-1	-1	+2
Mesh[T]Chain	-1	+0	+0	+2	+1	+1	-2	+3	+1	-0	-1	+2
Mesh[T][S]	-0	-2	-1	+2	+1	+1	+1	+2	+1	+1	+1	+2
Mesh[T][S][FP]	-3	+1	-1	-2	-2	-2	-3	+1	-2	-3	-5	-1
Mesh[T][S]Sparse	-2	+1	-0	-0	-0	+0	-1	-0	-1	-2	-1	+1
Step[T]Alt	-0	-2	-3	-1	-2	-3	-2	+6	-1	-3	-5	+1
Step[T][S]	-1	-2	-3	-1	-2	-3	-2	+6	-1	-3	-4	+1
Step[T][S][FP]	-2	-2	-3	-0	-2	-2	-2	+7	-0	-3	-3	+0
Step[T][S][HP]	-0	-2	-3	+0	-2	-2	-1	+7	-1	-3	-5	+1
Step[T][S][HP]Async	-1	-3	-3	-0	-2	-2	-2	+6	-0	-3	-4	+1
Step[T][S][L]	-2	-3	-3	+0	-3	-2	-1	+8	-2	-3	-3	+2
Step[T][S][L]Cache	-1	-3	-3	+1	-2	-3	-1	+6	-1	-3	-4	+2
Step[T][S]Sparse	-2	-2	-3	+0	-2	-2	-2	+6	-1	-3	-4	+1
[T]Alt	-0	-2	-1	+1	-0	-0	-1	+2	-0	-1	-1	+1
[T][S]	-0	-3	-2	+1	+0	+1	+0	+2	+1	+0	+1	+3
[T][S][FP]	-3	+1	-2	-1	-3	-2	-3	+0	-1	-3	-4	-0
[T][S][HP]	-3	-3	-1	-1	-2	-1	-2	-0	-2	-3	-5	+0
[T][S][HP]Async	+0	+0	+0	+1	-0	+0	+0	-0	+0	-0	-3	+2
[T][S][L]	-0	+1	-0	+1	+1	+1	+1	+0	+2	-0	-4	+3
[T][S][L]Cache	+1	+2	+2	+3	+3	+2	+2	-0	+2	+1	-4	+4
[T][S]Sparse	-1	+0	-0	-0	-1	-1	-1	+0	+0	-2	-1	+1
step_sgd	+0	-0	-0	-2	+1	-1	-1	+0	+1	-2	-1	+2
step_tween	-2	-2	-2	+0	-2	-2	-3	+6	+0	-2	-2	+1
step_tween_chain	-2	+1	-1	-0	-0	+0	-2	-0	-1	-2	-1	+3
tween	-1	-1	-2	-1	-1	-1	-2	+7	-1	-3	-3	+2
tween_chain	-1	+0	-1	-0	+0	+0	-1	+2	+0	-0	-0	+3

AccD vs sgd, every mode x dtype (cols 25-34)

AccD vs sgd, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	-0	+1	-3	-3	+1	+0	+0	+0	-0	+1
Mesh[T]	-0	-1	-3	-1	-2	-2	-2	+1	-1	-1
Mesh[T]Alt	+1	-0	-1	+0	-1	+0	-1	-0	-0	-0
Mesh[T]Chain	+1	+1	-2	+0	+0	-1	+0	+0	-2	-0
Mesh[T][S]	+1	+1	-1	+1	+1	+1	+1	+0	+1	+1
Mesh[T][S][FP]	-2	-1	-3	-2	-3	-3	-2	-2	-3	-2
Mesh[T][S]Sparse	-1	+1	-1	-1	-1	-1	-2	-2	-1	-1
Step[T]Alt	-1	-3	-4	-2	-4	-4	-2	-1	-0	-0
Step[T][S]	-0	-2	-3	-1	-3	-3	-2	-1	-1	-1
Step[T][S][FP]	-1	-2	-4	-1	-3	-3	-1	-1	-0	+0
Step[T][S][HP]	-0	-3	-3	-1	-3	-3	-2	-1	-0	+0
Step[T][S][HP]Async	+0	-2	-4	-1	-3	-3	-1	-1	-0	-0
Step[T][S][L]	+0	-3	-3	-2	-3	-3	-1	-1	-1	+1
Step[T][S][L]Cache	-0	-3	-4	-1	-3	-3	-2	-1	-1	+0
Step[T][S]Sparse	-1	-2	-4	-1	-2	-3	-2	-2	-1	+1
[T]Alt	-0	+0	-1	-1	-0	-0	-1	-0	-1	+1
[T][S]	+1	+1	+0	+0	+1	+0	+0	+0	+1	+1
[T][S][FP]	-2	-3	-3	-3	-3	-2	-2	-2	-2	-2
[T][S][HP]	-2	-2	-4	-3	-2	-3	-2	-2	-3	-2
[T][S][HP]Async	+0	-1	-1	-0	-1	-0	-0	-0	+0	+0
[T][S][L]	+0	-3	-1	+0	+0	+0	+0	+0	+1	+1
[T][S][L]Cache	+3	-4	+1	+2	+2	+1	+2	+1	+2	+2
[T][S]Sparse	-0	-0	-2	-0	-1	-1	-1	-1	-1	-1
step_sgd	+0	+0	-1	-1	-1	-0	-1	-2	-1	+1
step_tween	-1	-0	-3	-0	-2	-2	-2	-1	-0	-2
step_tween_chain	+0	+0	-1	-1	-0	-1	-0	-0	-2	-1
tween	+0	-1	-3	-1	-3	-3	-1	-0	-0	-1
tween_chain	+1	+1	-1	-0	+0	-2	+0	+0	+1	+2

ScoreD vs sgd, every mode x dtype (cols 1-12)

ScoreD vs sgd, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	-1	-1	-0	-0	-1	-2	-2	-1	-0	-1	-1	-1
Mesh[T]	+0	-4	+1	+0	+0	-0	+1	-1	-1	-0	-1	-0
Mesh[T]Alt	-3	-4	-2	-2	-2	-5	-3	-1	-1	-3	-2	-2
Mesh[T]Chain	-1	-0	-1	-2	-0	-3	-1	-0	-0	-2	-1	-0
Mesh[T][S]	-1	+1	-1	-1	-1	-4	-2	+3	+1	+1	-1	+1
Mesh[T][S][FP]	-2	-4	-1	-1	-1	-3	-1	+1	-0	-1	-1	-1
Mesh[T][S]Sparse	+3	+14	+1	+1	+2	+1	+2	+4	+2	+1	+2	+1
Step[T]Alt	-1	-5	-1	-1	-1	-3	-2	-1	-2	-2	-2	-1
Step[T][S]	+2	-4	+1	+2	+1	+1	+2	+0	-1	+2	+2	+1
Step[T][S][FP]	+1	-4	+2	+2	+2	+2	+2	-0	-1	+1	+1	+1
Step[T][S][HP]	+2	-4	+1	+1	+2	+2	+3	-0	-1	+1	+1	+2
Step[T][S][HP]Async	+2	-4	+2	+2	+2	+1	+2	-0	-1	+1	+0	+2
Step[T][S][L]	+6	-1	+5	+5	+8	+9	+7	+2	+1	+5	+6	+5
Step[T][S][L]Cache	+8	-1	+5	+5	+6	+10	+8	+2	+0	+4	+5	+7
Step[T][S]Sparse	+3	-4	+2	+2	+1	+1	+2	-0	-0	+0	+2	+2
[T]Alt	-2	-4	-2	-2	-2	-5	-3	-1	-1	-3	-3	-2
[T][S]	-1	+2	-1	-1	-1	-4	-1	+2	+1	+1	-2	+1
[T][S][FP]	-2	-3	-1	-1	-1	-4	-2	+1	-0	-1	-2	-1
[T][S][HP]	-2	-3	-1	-1	-1	-4	-2	+0	-0	-1	-1	-1
[T][S][HP]Async	-1	-1	-1	-1	-1	-4	-1	+1	+1	-1	-2	-1
[T][S][L]	+1	-0	+0	+5	+1	+2	+1	+4	+3	+5	+0	+1
[T][S][L]Cache	+1	+2	+1	+1	+1	-2	+2	+4	+5	+2	+0	+1
[T][S]Sparse	+1	+11	+1	+2	+1	+3	+2	+4	+2	+2	+1	+1
step_sgd	-1	+0	-1	-1	-1	-3	-1	+1	-0	-1	-1	-1
step_tween	+2	-4	+1	+2	+2	+1	+2	-0	-1	+1	-0	+1
step_tween_chain	-2	+0	-1	-1	-1	-3	-1	+0	+0	+1	-2	-1
tween	+1	-4	+0	+1	+1	+0	+1	-1	-1	-1	-1	+0
tween_chain	-1	-3	-0	-0	-2	-2	-0	-0	-0	-0	-2	-0

ScoreD vs sgd, every mode x dtype (cols 13-24)

ScoreD vs sgd, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	-1	-1	-0	-0	-1	-1	-0	+1	+0	-0	-2	+1
Mesh[T]	-2	-3	-2	-1	-4	-1	-1	+2	-3	-2	-5	-0
Mesh[T]Alt	-3	-4	-2	-3	-4	-1	-2	-1	-5	-3	-5	-1
Mesh[T]Chain	-1	-1	-0	+0	-1	+0	-1	+2	-0	-1	-2	+1
Mesh[T][S]	+1	-1	+0	+2	+2	+1	+1	+3	+3	+2	+2	+3
Mesh[T][S][FP]	-2	+2	+0	-0	-1	-0	-0	+1	-2	-1	-4	+0
Mesh[T][S]Sparse	+3	+15	+5	+5	+11	+4	+3	+3	+8	+3	+13	+6
Step[T]Alt	-3	-4	-2	-3	-4	-2	-2	+1	-5	-3	-6	-1
Step[T][S]	-1	-2	-1	-1	-3	-1	-1	+4	-2	-2	-4	+0
Step[T][S][FP]	-2	-2	-1	-0	-3	-1	-1	+4	-1	-2	-4	+0
Step[T][S][HP]	-1	-3	-2	-0	-3	-1	-1	+4	-2	-2	-6	+0
Step[T][S][HP]Async	-1	-3	-1	-0	-2	-1	-1	+4	-1	-2	-4	+1
Step[T][S][L]	+1	+1	-1	+2	+0	-0	+1	+9	+1	-0	+0	+3
Step[T][S][L]Cache	+1	+0	-0	+3	+2	-0	+1	+8	+3	-1	-1	+4
Step[T][S]Sparse	-2	-3	-2	-0	-3	-1	-1	+3	-2	-2	-4	+0
[T]Alt	-3	-5	-2	-2	-4	-1	-2	-0	-5	-3	-5	-1
[T][S]	+1	-2	+0	+2	+1	+1	+1	+3	+3	+1	+3	+3
[T][S][FP]	-2	+2	-0	-0	-2	-0	-0	+1	-1	-1	-4	+1
[T][S][HP]	-2	-3	+1	+0	-2	+0	-0	+0	-2	-1	-4	+1
[T][S][HP]Async	+2	+1	+1	+2	+1	+1	+1	+0	+1	+1	-2	+2
[T][S][L]	+6	+12	+4	+7	+14	+3	+4	+3	+13	+5	-0	+8
[T][S][L]Cache	+9	+20	+7	+10	+23	+6	+5	+3	+19	+8	+3	+12
[T][S]Sparse	+5	+14	+5	+5	+10	+3	+3	+3	+11	+3	+12	+6
step_sgd	+2	+1	+1	-0	+2	+0	+0	+1	+3	-0	+0	+3
step_tween	-2	-2	-1	-0	-3	-1	-1	+4	-1	-1	-3	+0
step_tween_chain	-1	+2	+0	+1	+0	+1	-0	+0	-0	-1	+0	+3
tween	-2	-2	-2	-2	-3	-1	-1	+3	-3	-2	-5	-0
tween_chain	-1	-1	-0	-1	-0	+0	-0	+1	-1	-0	-1	+1

ScoreD vs sgd, every mode x dtype (cols 25-34)

ScoreD vs sgd, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	-1	+0	-2	-3	-0	-0	-0	-0	-2	-0
Mesh[T]	-2	-2	-2	-3	-3	-1	-1	-1	-3	-2
Mesh[T]Alt	-3	-3	-2	-3	-3	-2	-2	-3	-5	-2
Mesh[T]Chain	-0	-0	-2	-1	-0	-1	-0	-1	-3	-1
Mesh[T][S]	+2	+2	+1	+2	+2	+1	+1	+2	+2	+2
Mesh[T][S][FP]	-1	-0	-1	-1	-1	-0	-0	-1	-2	-0
Mesh[T][S]Sparse	+5	+8	+4	+5	+5	+3	+2	+4	+10	+4
Step[T]Alt	-3	-3	-3	-4	-4	-2	-2	-3	-5	-2
Step[T][S]	-1	-2	-2	-1	-2	-1	-1	-1	-2	-1
Step[T][S][FP]	-0	-2	-2	-1	-2	-1	-1	-1	-2	-0
Step[T][S][HP]	-1	-2	-2	-2	-3	-1	-1	-1	-2	-0
Step[T][S][HP]Async	-0	-1	-2	-2	-2	-1	-0	-1	-2	-0
Step[T][S][L]	+3	-0	-0	+1	-0	-0	+1	+2	+3	+3
Step[T][S][L]Cache	+2	-0	-1	+1	-0	+0	+0	+2	+2	+3
Step[T][S]Sparse	-1	-2	-2	-2	-2	-1	-1	-1	-2	+0
[T]Alt	-3	-3	-2	-4	-3	-2	-2	-3	-5	-2
[T][S]	+2	+2	+1	+1	+2	+1	+1	+2	+2	+2
[T][S][FP]	-1	-2	-1	-1	-1	-0	-0	-0	-2	-0
[T][S][HP]	-0	-1	-1	-2	-1	-1	-0	-1	-3	-0
[T][S][HP]Async	+1	+0	+0	+1	+0	+1	+1	+1	+1	+1
[T][S][L]	+7	+1	+3	+8	+7	+4	+3	+8	+9	+6
[T][S][L]Cache	+12	-0	+7	+12	+12	+6	+6	+10	+18	+10
[T][S]Sparse	+7	+7	+3	+7	+7	+3	+3	+5	+8	+4
step_sgd	+2	+2	+1	+0	+0	+1	+0	+0	-0	+1
step_tween	-1	-1	-2	-1	-2	-1	-1	-1	-1	-1
step_tween_chain	+1	+1	+0	-0	+1	+0	+1	+1	-1	+0
tween	-1	-1	-2	-2	-3	-2	-1	-2	-3	-2
tween_chain	+0	+0	-1	-1	-0	-1	-0	+0	-0	+0

AvailD vs sgd, every mode x dtype (cols 1-12)

AvailD vs sgd, every mode x dtype (cols 1-12)

	bfloat16	binary	complex128	complex64	float16	float32	float64	fp4	fp6	fp8e4m3	fp8e5m2	int
MeshBP	-1	-0	-1	-1	-1	-1	-0	-1	+0	-1	-0	-0
Mesh[T]	-3	-3	-3	-3	-3	-4	-2	-3	-3	-3	-2	-4
Mesh[T]Alt	-0	-8	-2	-1	-0	-1	-1	-9	-8	-8	-1	-6
Mesh[T]Chain	-1	-0	-1	-1	-1	-1	-0	-1	+0	-1	+0	-0
Mesh[T][S]	+3	+4	+4	+4	+4	+2	+4	+3	+4	+4	+4	+5
Mesh[T][S][FP]	+4	+3	+4	+4	+4	+3	+4	+3	+5	+4	+4	+4
Mesh[T][S]Sparse	+13	+14	+11	+12	+13	+12	+12	+13	+13	+12	+13	+12
Step[T]Alt	-7	-8	-7	-7	-7	-7	-6	-7	-7	-7	-7	-7
Step[T][S]	+0	+1	-0	+0	+0	-1	+1	-0	+1	+1	+0	+0
Step[T][S][FP]	-0	-0	+0	+1	-0	-1	+0	+0	+0	+1	-0	+0
Step[T][S][HP]	-1	-1	-1	-0	-0	-1	+0	-0	-1	-0	-1	-0
Step[T][S][HP]Async	+0	+1	+0	+1	+0	-1	+1	+0	+0	+1	+0	+0
Step[T][S][L]	+7	+8	+6	+6	+7	+6	+7	+7	+6	+7	+6	+5
Step[T][S][L]Cache	+7	+8	+6	+6	+7	+6	+7	+7	+6	+7	+6	+6
Step[T][S]Sparse	+0	+0	+0	+0	+0	-1	+0	-0	+1	+1	+1	+0
[T]Alt	+0	-8	-2	-1	-0	-1	-1	-8	-9	-8	-1	-6
[T][S]	+3	+4	+4	+4	+4	+2	+4	+3	+5	+3	+4	+4
[T][S][FP]	+3	+3	+4	+5	+4	+2	+4	+3	+5	+4	+4	+4
[T][S][HP]	+3	+4	+4	+4	+4	+2	+4	+3	+5	+4	+4	+4
[T][S][HP]Async	+3	+4	+4	+4	+4	+2	+4	+3	+5	+4	+4	+4
[T][S][L]	+11	+10	+11	+12	+12	+12	+12	+13	+11	+11	+12	+12
[T][S][L]Cache	+12	+14	+11	+12	+12	+12	+13	+13	+13	+13	+12	+13
[T][S]Sparse	+12	+14	+11	+12	+12	+12	+13	+13	+13	+12	+13	+12
step_sgd	+3	+3	+3	+3	+3	+3	+5	+3	+4	+4	+4	+4
step_tween	-0	-2	-1	+0	+0	-1	+1	-1	-0	-0	-0	-0
step_tween_chain	+3	+2	+3	+2	+3	+2	+4	+3	+4	+3	+4	+3
tween	-2	-3	-3	-3	-3	-3	-2	-2	-3	-3	-3	-3
tween_chain	-1	+0	-1	-0	-0	-1	+1	-1	-0	-0	+0	-0

AvailD vs sgd, every mode x dtype (cols 13-24)

AvailD vs sgd, every mode x dtype (cols 13-24)

	int16	int2	int3	int32	int4	int5	int6	int64	int8	nf4	ternary	uint
MeshBP	-0	-1	-1	-0	-1	-1	-0	-0	-0	-0	-1	-1
Mesh[T]	-3	-3	-4	-3	-3	-3	-4	-3	-3	-4	-3	-4
Mesh[T]Alt	-9	-8	-8	-8	-8	-8	-9	-6	-9	-8	-9	-9
Mesh[T]Chain	-1	-1	-1	-0	-1	+0	-0	-0	-0	-1	-1	-1
Mesh[T][S]	+4	+3	+4	+4	+3	+4	+4	+4	+3	+3	+2	+4
Mesh[T][S][FP]	+4	+3	+4	+4	+3	+5	+5	+5	+2	+4	+3	+4
Mesh[T][S]Sparse	+12	+14	+13	+12	+14	+13	+12	+12	+12	+12	+14	+12
Step[T]Alt	-7	-7	-7	-7	-7	-7	-7	-7	-7	-7	-8	-8
Step[T][S]	+0	-0	+0	+0	+0	+0	+0	+0	-0	+0	+0	+0
Step[T][S][FP]	-0	-1	-0	+0	-1	+0	+0	+0	-1	-0	-1	-0
Step[T][S][HP]	-1	-2	-1	-1	-1	-0	-1	+0	-1	-1	-3	-1
Step[T][S][HP]Async	+1	-0	-0	+0	+0	-0	+0	+0	-1	-0	-0	+0
Step[T][S][L]	+6	+8	+5	+6	+8	+6	+6	+6	+7	+5	+8	+6
Step[T][S][L]Cache	+6	+7	+6	+5	+8	+6	+5	+7	+7	+5	+7	+6
Step[T][S]Sparse	+0	-0	+0	-0	-0	+0	+0	+0	-1	+0	-1	-0
[T]Alt	-9	-8	-9	-9	-8	-8	-8	-6	-8	-9	-9	-9
[T][S]	+4	+2	+4	+4	+3	+5	+4	+5	+3	+4	+3	+4
[T][S][FP]	+3	+3	+4	+4	+3	+5	+4	+5	+3	+4	+2	+4
[T][S][HP]	+4	+3	+4	+4	+3	+5	+4	+5	+3	+5	+3	+4
[T][S][HP]Async	+4	+3	+4	+4	+3	+4	+4	+5	+3	+4	+3	+4
[T][S][L]	+11	+12	+10	+11	+12	+10	+11	+13	+11	+11	+9	+11
[T][S][L]Cache	+12	+14	+12	+12	+14	+12	+13	+13	+13	+12	+13	+13
[T][S]Sparse	+11	+14	+12	+12	+14	+12	+12	+12	+12	+12	+14	+12
step_sgd	+4	+2	+3	+4	+3	+4	+4	+5	+3	+3	+3	+4
step_tween	-0	-1	-1	-0	-2	-1	-1	+0	-1	-1	-1	-1
step_tween_chain	+3	+2	+3	+3	+2	+3	+4	+4	+3	+3	+2	+3
tween	-3	-3	-3	-3	-3	-3	-3	-3	-3	-3	-4	-3
tween_chain	+0	-0	-0	-0	-0	-0	-0	+0	-1	-0	-1	-0

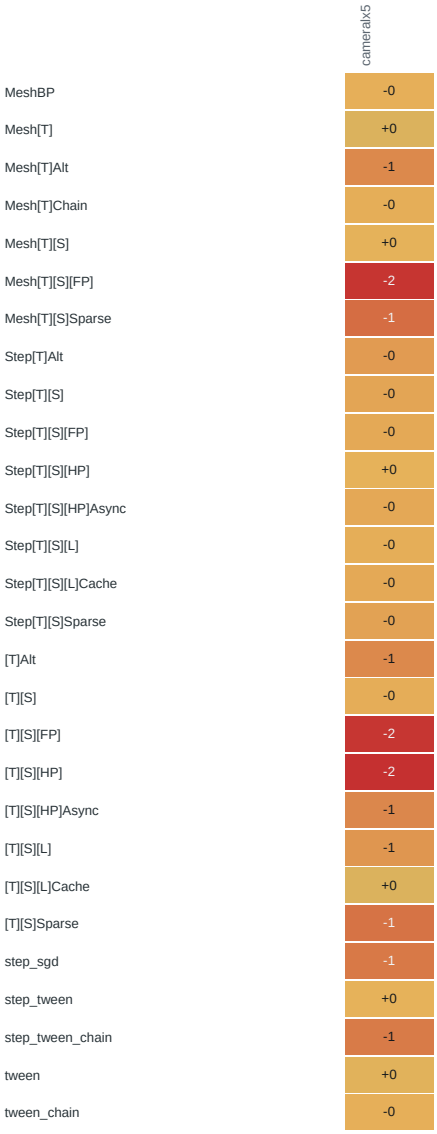
AvailD vs sgd, every mode x dtype (cols 25-34)

AvailD vs sgd, every mode x dtype (cols 25-34)

	uint16	uint2	uint3	uint32	uint4	uint5	uint6	uint64	uint8	uintptr
MeshBP	-0	-0	-1	-1	-1	-1	-0	-1	-1	-1
Mesh[T]	-3	-3	-4	-4	-3	-3	-4	-3	-4	-4
Mesh[T]Alt	-8	-8	-9	-9	-9	-8	-8	-9	-9	-9
Mesh[T]Chain	-0	-1	-1	-1	-1	-1	-0	-0	-1	-1
Mesh[T][S]	+4	+4	+3	+3	+4	+4	+4	+4	+3	+3
Mesh[T][S][FP]	+4	+4	+4	+3	+4	+5	+4	+4	+3	+3
Mesh[T][S]Sparse	+12	+13	+12	+12	+12	+13	+13	+12	+13	+12
Step[T]Alt	-7	-7	-8	-7	-7	-7	-8	-7	-7	-7
Step[T][S]	+0	-0	-0	-0	-0	+0	+0	+0	-0	-0
Step[T][S][FP]	+1	-0	-0	-1	+0	+0	-0	+0	-1	-0
Step[T][S][HP]	-0	-0	-1	-1	-1	-1	-1	-0	-1	-1
Step[T][S][HP]Async	+0	+0	-1	-1	-0	+0	+0	+0	-1	-0
Step[T][S][L]	+7	+6	+6	+6	+7	+6	+6	+7	+6	+6
Step[T][S][L]Cache	+7	+6	+6	+6	+6	+6	+6	+7	+6	+6
Step[T][S]Sparse	+1	-0	-0	-0	+0	+0	+0	-0	-1	-0
[T]Alt	-8	-9	-9	-9	-9	-9	-9	-8	-9	-9
[T][S]	+5	+4	+3	+3	+4	+5	+4	+4	+3	+3
[T][S][FP]	+4	+4	+4	+3	+4	+4	+5	+4	+3	+4
[T][S][HP]	+4	+4	+4	+3	+4	+4	+4	+4	+3	+4
[T][S][HP]Async	+4	+3	+3	+4	+3	+5	+5	+4	+3	+4
[T][S][L]	+12	+11	+10	+11	+11	+11	+10	+12	+10	+11
[T][S][L]Cache	+13	+12	+12	+12	+13	+13	+13	+13	+12	+12
[T][S]Sparse	+13	+13	+12	+12	+12	+13	+13	+12	+12	+11
step_sgd	+4	+3	+3	+3	+3	+4	+3	+4	+3	+3
step_tween	+0	-1	-1	-1	-0	-1	-1	+0	-1	-1
step_tween_chain	+3	+3	+3	+3	+3	+3	+3	+3	+3	+3
tween	-3	-3	-3	-3	-3	-3	-3	-3	-3	-3
tween_chain	+0	-0	-0	-1	-0	-0	-0	+0	+0	-1

AccD vs sgd, every mode x arch

AccD vs sgd, every mode x arch



Family collapse - Step* vs non-Step

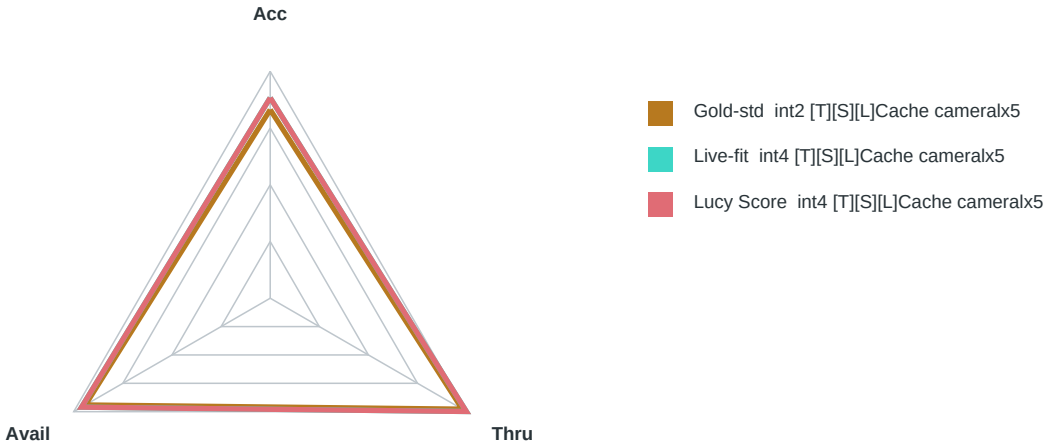
Step* is a 1D pipe (one sample enters layer 0 per tick; output is the sample that entered depth ticks ago). Non-Step of the same family is a full-chain update. AccD is a real scheduler split, not leftover warm-up forwards.

step	plain	n	mean |AccD|
Step[T]Alt	[T]Alt	34	2.82
Step[T][S]	[T][S]	34	3.14
Step[T][S][FP]	[T][S][FP]	34	2.45
Step[T][S][HP]	[T][S][HP]	34	2.62
Step[T][S][HP]Async	[T][S][HP]Async	34	2.76
Step[T][S][L]	[T][S][L]	34	2.96
Step[T][S][L]Cache	[T][S][L]Cache	34	3.93
Step[T][S]Sparse	[T][S]Sparse	34	2.59
step_sgd	sgd	34	1.35
step_tween	tween	34	0.66
step_tween_chain	tween_chain	34	1.26

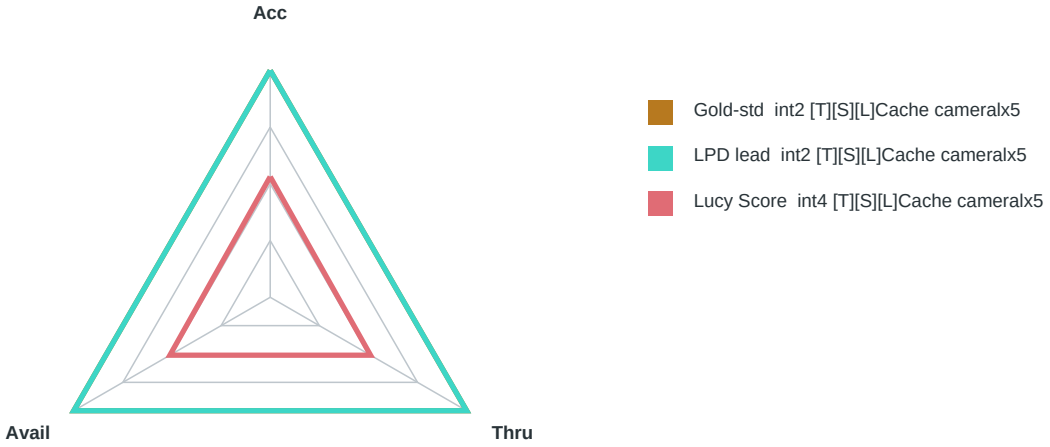
Consciousness - Acc, Throughput, Availability

Synthetic organism / Lucy density: can the net run and train at the same time in a small box. Lucy Score = Throughput x Availability x Acc / 10,000 (hard Acc; SoftAcc is serve-confidence only). SGD that blocks serve dies on Availability. Q = geomean Acc/Thru/Avail vs learner peaks (traps do not set Thru/Avail). LPD = Q x shrink vs Acc-champ RAM; 0 unless Acc keep >=70%. Gold = all 3 pillars >=80% at <=20% Acc-champ RAM. Gold-std = Acc >=80% plus Thru or Avail, then smallest then fastest. Score/MiB is the binary trap.
Acc champ int64|none|Step[T][S][L]|cameralx5|simd Acc 10.6 Thru 330 Avail 30.2% 752.8 KiB (RAM reference)
Lucy Score champ (T x Avail x Acc) int4|none|[T][S][L]Cache|cameralx5|simd Score 28.8 Acc 9.4 Soft 5 47.0 KiB
Live-fit champ (best Q) int4|none|[T][S][L]Cache|cameralx5|simd Acc 9.4 Thru 858 Avail 35.8% 47.0 KiB
Gold-std (2+ pillars, Acc keep >= 80%, then smallest then fastest): int2|none|[T][S][L]Cache|cameralx5|simd mode [T][S][L]Cache Acc 8.8 Thru 840 23.5 KiB
Board fastest float32|none|[T][S][L]|cameralx5|simd Thru 917 (traps may own this) Best availability fp6|none|[T][S][L]Cache|cameralx5|simd 37.3%
Learner Thru peak 859 learner Avail peak 37.3%

Consciousness radar - Acc / Thru / Avail vs learner peaks



Memory density radar - same pillars x shrink vs Acc champ (traps sit at origin)



Gold - trifecta >=80% at <=20% of Acc-champ RAM

Band	Cell	Acc%	Thru%	Avail%	Q%	RAM%	xSmall	LPD	Acc	Thru	KiB
gold	int2 [T][S][L]Cache cameralx5	83	98	94	91	3	32.0	29.26	8.8	840	23.5
gold	int4 [T][S][L]Cache cameralx5	88	100	96	95	6	16.0	15.14	9.4	858	47.0

gold	uint8 [T][S][L]Cache cameralx5	83	91	98	91	13	8.0	7.24	8.8	785	94.1

Gold-standard train modes - 2+ pillars, Acc keep >= 80%, smallest then fastest

Mode	n	Acc	KiB	Thru	Cell
[T][S][L]Cache	7	9.4	23.5	858	int2 [T][S][L]Cache cameralx5 / int4 [T][S][L]Cache cameralx5
Step[T][S][L]	5	10.6	94.1	402	fp8e4m3 Step[T][S][L] cameralx5 / float16 Step[T][S][L] cameralx5
Step[T][S][L]Cache	5	10.0	752.8	494	float64 Step[T][S][L]Cache cameralx5

Near-gold - 2+ pillars, RAM <= 50% of Acc champ

Band	Cell	Acc%	Thru%	Avail%	Q%	RAM%	xSmall	LPD	Acc	Thru	KiB
near	uint3 [T][S][L]Cache cameralx5	81	39	99	68	5	21.3	14.50	8.6	338	35.3
near	uint4 [T][S][L]Cache cameralx5	80	61	99	79	6	16.0	12.56	8.5	527	47.1
near	fp8e4m3 Step[T][S][L] cameralx5	84	38	82	64	12	8.0	5.12	8.9	324	94.1
near	float16 Step[T][S][L] cameralx5	92	47	83	71	25	4.0	2.83	9.7	402	188.2

Lucy density (LPD) - Q x shrink vs Acc-champ RAM; 0 if Acc keep < 70%

Band	Cell	Acc%	Thru%	Avail%	Q%	RAM%	xSmall	LPD	Acc	Thru	KiB
gold	int2 [T][S][L]Cache cameralx5	83	98	94	91	3	32.0	29.26	8.8	840	23.5
-	ternary [T][S] cameralx5	77	55	66	66	3	32.0	20.99	8.2	475	23.5
-	ternary Mesh[T][S] cameralx5	77	53	64	64	3	32.0	20.47	8.1	456	23.5
gold	int4 [T][S][L]Cache cameralx5	88	100	96	95	6	16.0	15.14	9.4	858	47.0
near	uint3 [T][S][L]Cache cameralx5	81	39	99	68	5	21.3	14.50	8.6	338	35.3
-	int3 [T][S][L]Cache cameralx5	79	38	99	67	5	21.3	14.20	8.4	322	35.3
-	int4 [T][S][L] cameralx5	70	90	91	83	6	16.0	13.34	7.5	775	47.0
near	uint4 [T][S][L]Cache cameralx5	80	61	99	79	6	16.0	12.56	8.5	527	47.1
-	nf4 [T][S][L]Cache cameralx5	76	45	96	69	6	16.0	11.09	8.1	391	47.0
-	uint3 [T][S] cameralx5	71	25	75	51	5	21.3	10.87	7.6	213	35.3
-	uint4 Mesh[T][S] cameralx5	72	39	75	59	6	16.0	9.47	7.6	332	47.1
-	uint4 MeshBP cameralx5	71	30	63	51	6	16.0	8.21	7.5	260	47.1
-	uint5 [T][S][L]Cache cameralx5	73	33	99	62	8	12.8	7.91	7.8	282	58.9
-	int5 [T][S][L]Cache cameralx5	75	31	98	61	8	12.8	7.81	8.0	264	58.8
-	int8 [T][S][L]Cache cameralx5	77	100	96	91	12	8.0	7.24	8.2	859	94.1
gold	uint8 [T][S][L]Cache cameralx5	83	91	98	91	13	8.0	7.24	8.8	785	94.1
-	int8 [T][S][L] cameralx5	71	91	90	83	12	8.0	6.67	7.5	779	94.1
-	uint6 [T][S][L]Cache cameralx5	76	30	100	61	9	10.7	6.52	8.1	259	70.6
-	int6 [T][S][L]Cache cameralx5	78	28	99	60	9	10.7	6.44	8.3	243	70.6
-	fp6 [T][S][L]Cache cameralx5	74	29	100	60	9	10.7	6.36	7.9	245	70.6

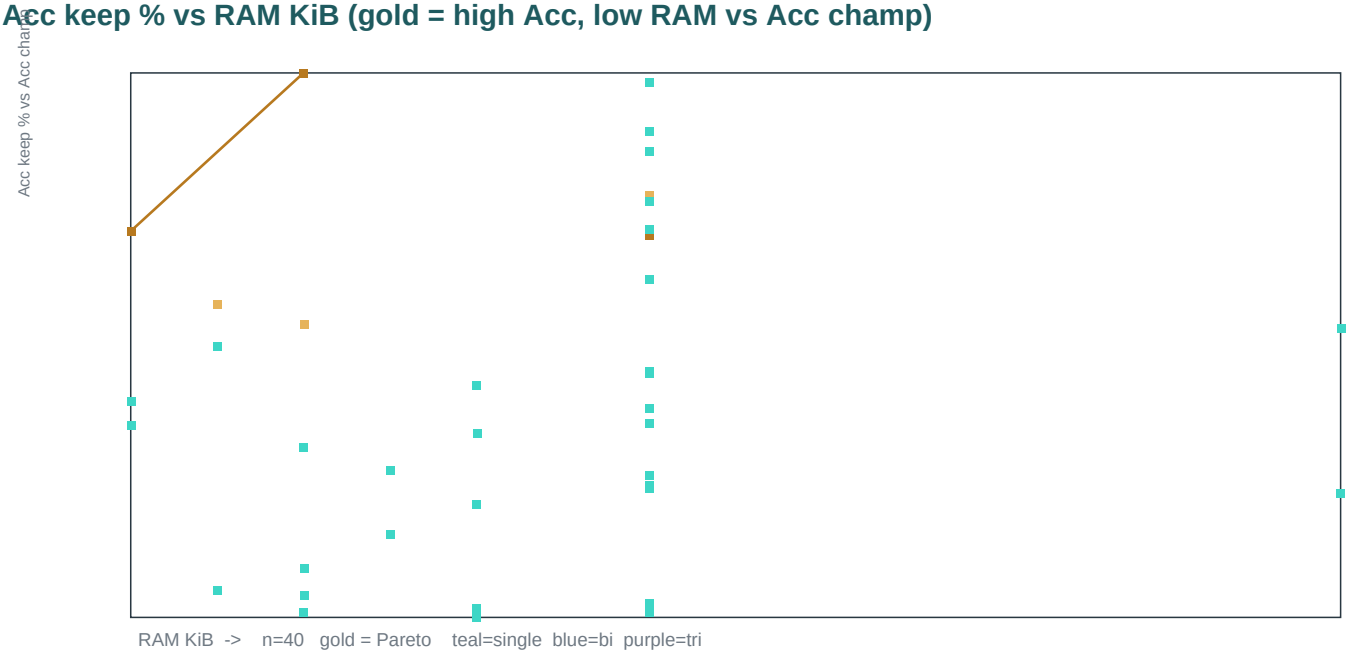
Consciousness rank - Q = geomean Acc/Thru/Avail keep

Band	Cell	Acc%	Thru%	Avail%	Q%	LPD	Thru	Avail
gold	int4 [T][S][L]Cache cameralx5	88	100	96	95	15.14	858	35.8
gold	int2 [T][S][L]Cache cameralx5	83	98	94	91	29.26	840	35.1
-	int8 [T][S][L]Cache cameralx5	77	100	96	91	7.24	859	35.8
gold	uint8 [T][S][L]Cache cameralx5	83	91	98	91	7.24	785	36.4
-	int4 [T][S][L] cameralx5	70	90	91	83	13.34	775	34.0
-	int8 [T][S][L] cameralx5	71	91	90	83	6.67	779	33.7
acc	float32 Step[T][S][L]Cache cameralx5	88	74	79	80	1.60	634	29.6
keep	uint32 [T][S][L]Cache cameralx5	84	61	99	80	1.60	528	36.8
-	uint16 [T][S][L]Cache cameralx5	80	62	99	79	3.14	530	36.8
near	uint4 [T][S][L]Cache cameralx5	80	61	99	79	12.56	527	36.8

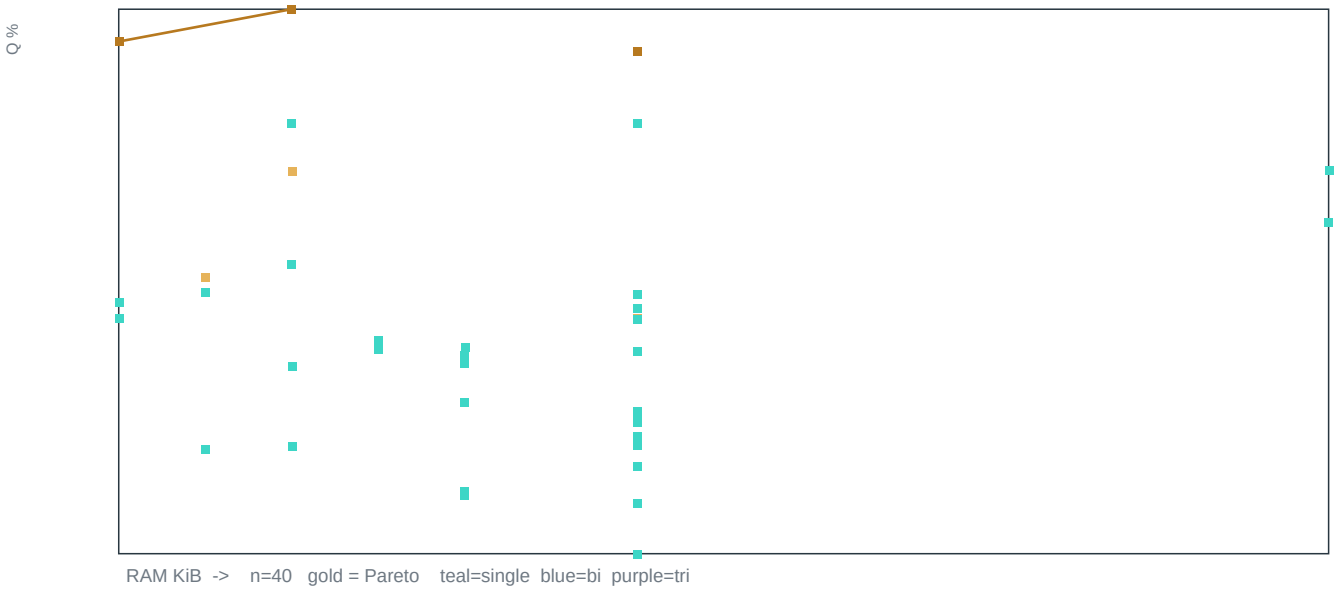
Trap - tiny RAM, Acc keep < 70% (Score/MiB and SoftAcc Score lie here)

Band	Cell	Acc%	Thru%	Avail%	Q%	RAM%	xSmall	LPD	Acc	Thru	KiB
trap	binary sgd cameralx5	62	49	57	56	2	32.0	0.00	6.6	419	11.8
trap	binary step_sgd cameralx5	51	55	64	56	2	32.0	0.00	5.4	472	11.8
trap	binary tween cameralx5	30	36	48	37	2	32.0	0.00	3.2	305	11.8
trap	binary tween_chain cameralx5	29	45	57	42	2	32.0	0.00	3.1	387	11.8
trap	binary step_tween cameralx5	29	39	53	39	2	32.0	0.00	3.1	336	11.8
trap	binary step_tween_chain cameralx5	55	51	63	56	2	32.0	0.00	5.8	442	11.8
trap	binary MeshBP cameralx5	61	44	56	53	2	32.0	0.00	6.5	376	11.8
trap	binary Mesh[T] cameralx5	30	36	49	38	2	32.0	0.00	3.2	305	11.8
trap	binary Mesh[T]Chain cameralx5	65	43	56	54	2	32.0	0.00	6.9	373	11.8
trap	binary [T][S] cameralx5	66	53	66	61	2	32.0	0.00	7.0	452	11.8

Acc keep % vs RAM KiB (gold = high Acc, low RAM vs Acc champ)

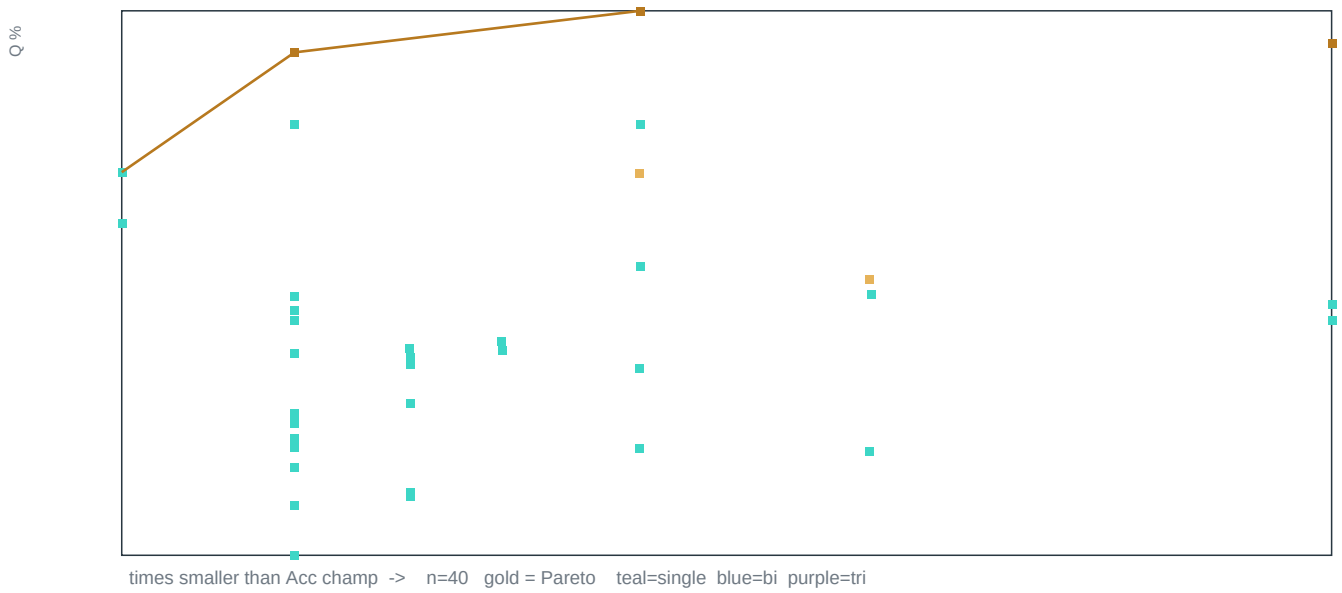


Q% vs RAM KiB (gold = high consciousness, low RAM)

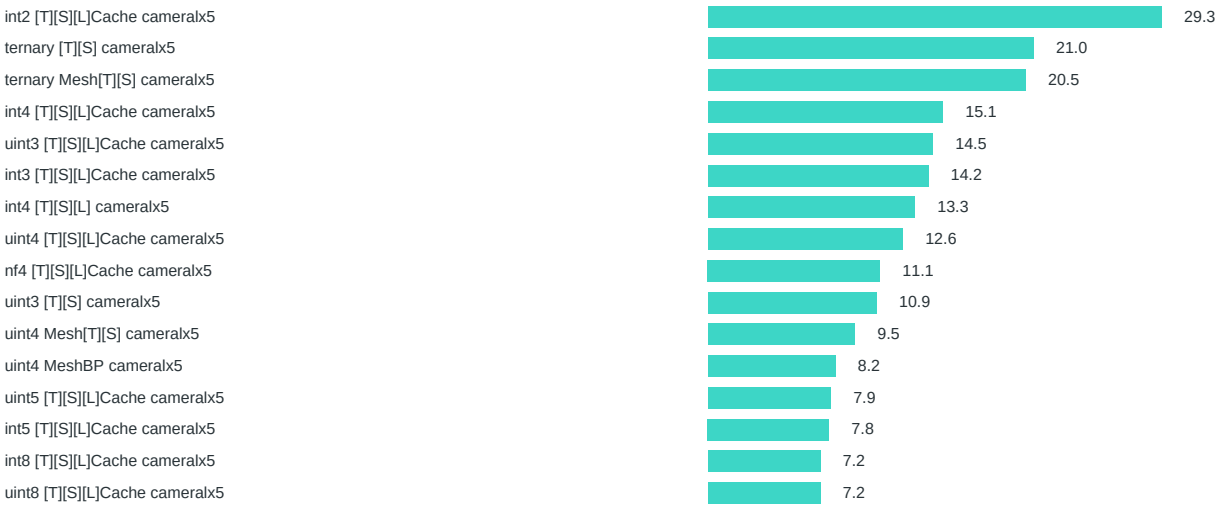


Q% vs shrink vs Acc champ (gold = upper right)

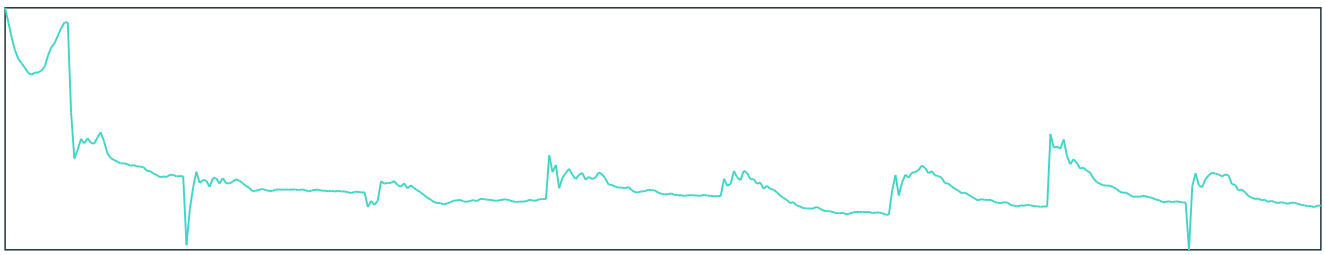
Q% vs shrink vs Acc champ (gold = upper right)



Top Lucy density (LPD)

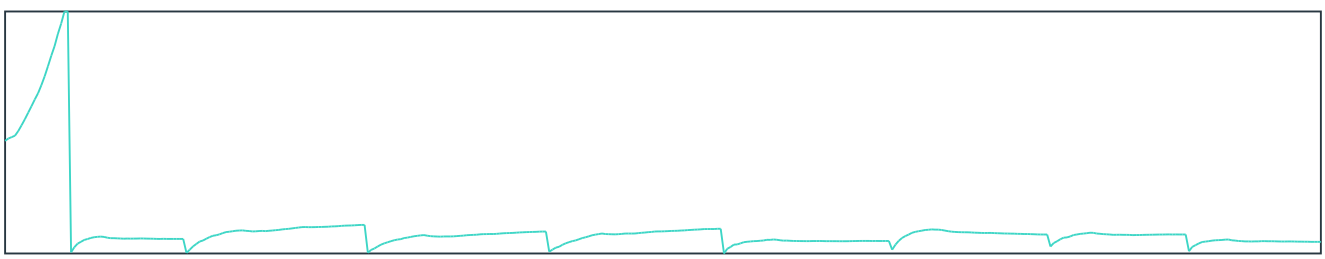


Live pulse (Score)



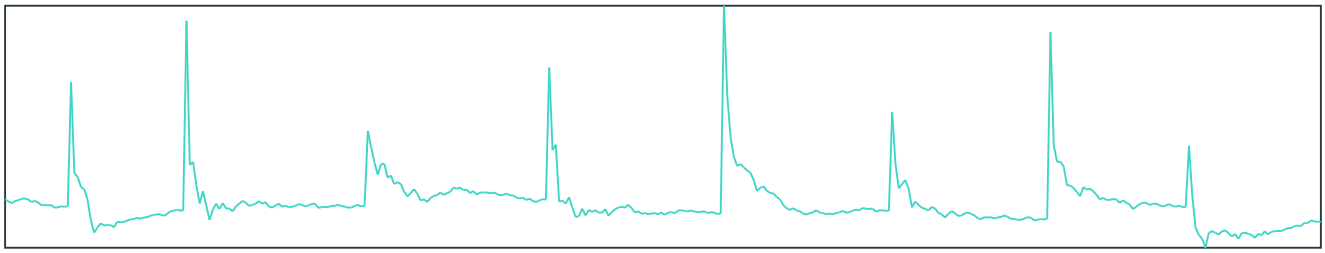
n=400 min=0.54 max=5.24

Live pulse (SoftAcc)



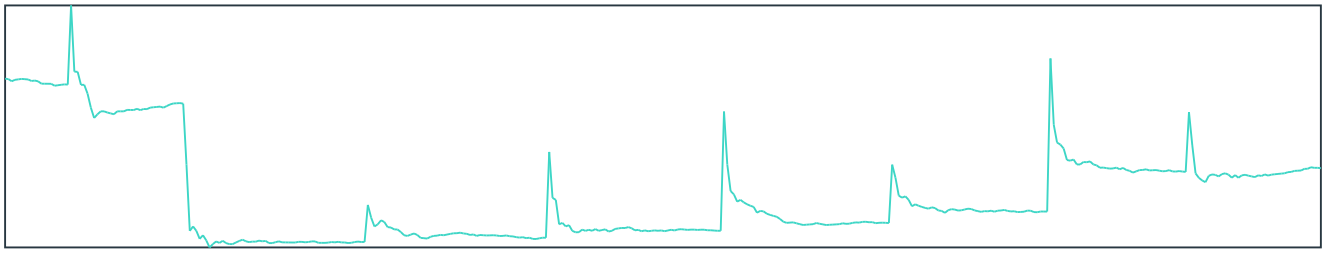
n=400 min=1.54 max=1.63

Live pulse (Availability)



n=400 min=23.22 max=31.93

Live pulse (Throughput)



n=400 min=125.99 max=271.81

Queue by train mode (this epoch)

Mode	Done	Run	Left	Total
sgd	34	0	0	34
step_sgd	34	0	0	34
tween	34	0	0	34
tween_chain	34	0	0	34
step_tween	34	0	0	34
step_tween_chain	34	0	0	34
MeshBP	34	0	0	34
Mesh[T]	34	0	0	34
Mesh[T]Chain	34	0	0	34
[T][S]	34	0	0	34
Step[T][S]	34	0	0	34
[T]Alt	34	0	0	34
Step[T]Alt	34	0	0	34
[T][S][HP]	34	0	0	34
[T][S][L]	34	0	0	34
[T][S][FP]	34	0	0	34
[T][S][L]Cache	34	0	0	34
[T][S][HP]Async	34	0	0	34
[T][S]Sparse	34	0	0	34
Mesh[T][S]	34	0	0	34
Mesh[T]Alt	34	0	0	34
Mesh[T][S][FP]	34	0	0	34
Mesh[T][S]Sparse	34	0	0	34
Step[T][S][HP]	34	0	0	34
Step[T][S][L]	34	0	0	34
Step[T][S][FP]	34	0	0	34
Step[T][S][L]Cache	34	0	0	34
Step[T][S][HP]Async	34	0	0	34

Step[T][S]Sparse	34	0	0	34